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矽晶片以熱音波能量直接覆晶接合於軟性基板銅電極之製程開發與機理研究
研究成果報告(精簡版)

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單一金球凸塊與軟性基板之熱音波接合機理分析

Analysis on Thermosonic Bonding Mechanism for a Single Ball Bumps Directly Bonding to the Flex Substrates

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一、中文摘要

本研究以熱音波銲線製程，將金球銲點銲著於鍍著鎳層與未鍍著鎳膜之軟性基板銅電極上，隨後再鍍著銀層作為金球銲點與軟板銅電極之接著層，避免金球銲點與軟板銅電極於熱音波銲線製程中，因銅電極氧化而危害其接合品質。鍍著鎳層於軟板銅電極之目的在於提高軟板銅電極之剛性，進而提升超音波功率(ultrasonic power)**於熱音波銲線製程之效率，有助於提升熱音波銲線製程之金球銲點與軟性基板銅電極之銲著強度**(bonding strength)**與銲著率**(bondability)**。**

實驗結果得知金球銲點與軟性基板銅電極之銲著率及銲著強度隨鎳膜鍍層的厚度增加而上升，軟性基板銅電極經鍍著厚度0.5 μm**鎳膜時，銲著率可達**100%**，且銲著強度高於**JEDEC**規範要求。經由金球銲點銲著面觀察發現，在相同的製程參數下，金球銲點與軟性基板接合時所產生摩擦痕跡隨鎳鍍膜層厚度的上升而增加，證實鎳層有效提升軟性基板之剛性，使超音波功率有效傳遞至接合界面。觀察推球剪力測試後之破斷面，發現金球銲點與具鎳鍍膜層之軟性基板的破壞模式為金球銲點連同銀/鎳鍍膜被剝離，顯示金球銲點與銀膜接著層之銲著強度高於鎳膜與銅電極之鍍層接合強度，且該強度高於**JEDEC**規範之要求。接合後之試片經高溫儲存測試後，得知隨持溫時間增加，銲著強度明顯上升，觀察接合界面，並未發現任何空孔或脫層等缺陷存在，顯示金球銲點銲著在具鎳鍍膜層之軟性基板並無高溫儲存可靠度之疑慮。鍍著適當厚度之鎳膜於軟板銅電極上，可提升軟板銅電極之剛性，並有助於傳遞熱音波銲線製程之超音波功率至金球與軟板銅電極之接合介面，進而提升金球銲點與軟板銅電極之接著率與接著強度。**

關鍵字： 熱音波銲線製程、軟性基板、鎳層

二、英文摘要

To improve the bondability and bonding strength for the gold wire thermosonic bonding to copper electrodes over the flex substrates, the nickel film was deposited on the surface of copper electrodes to strengthen their stiffness. A silver layer was then deposited on the nickel layer to prevent copper electrodes from oxidizing during thermosonic wire bonding process. The nickel layer was expected to improve the rigidity of the copper electrodes over flex substrates, increasing the efficiency of bonding of ultrasonic power.

According with the experimental results, the bondability and bonding strength increased with the thickness of nickel layer increased under the same bonding parameters. One hundred percent bondability and high bonding strength can be obtained when gold balls bonding to copper electrodes with depositing 0.5μm nickel layer. The bonding strength was higher than that stated in JEDEC stands. The bonding morphology of the gold ball exhibited an extensive bonded area with aligned traces if thermosonic wire bonding was conducted for gold ball bonding to copper electrodes with the nickel layer, while gold ball bonding to copper electrodes without depositing nickel layer resulted in a blank surface morphology. This observation on the bonding morphology of gold balls can be used to explain that nickel layer was effective in promoting rigidity of copper electrodes, increasing the efficiency of bonding of ultrasonic power. With deposition of the nickel layer onto copper electrodes, a layer stuck on the gold ball can be observed at the fractured morphology of gold ball, implying the bonding strength of gold ball bonded on copper electrodes was even higher

than adhesive strength of the layers deposited on the copper electrodes. The reliability of high temperature storage also verified in this study. The bonding strength of gold ball bonded on copper electrodes with a nickel layer deposition increased with extending storage period of HTS. The increased bonding strength was contributed to atomic interdiffusion between gold balls and copper electrodes. No delamination or any defect was found at bonding interface between gold ball and copper electrodes. Thus, the reliability of the gold ball bonding to copper electrodes with a nickel layer deposition is not a concern.

Deposition of 0.5μm nickel layer on copper electrodes over the flex substrates, the rigidity of copper electrodes was improved, and the ultrasonic power can be propagated to bonding interface between gold balls and copper electrodes in which results in bonding strength increasing.

Keywords: **Thermosonic wire bonding, nickel layer, flex substrate**

三、文獻回顧

隨著電子科技產業之蓬勃發展與進步，消費性電子產品之發展趨勢邁向輕、薄、短、小與易攜帶等功能，特別針對攜帶式通訊產品之要求日益增加，為滿足電子產品之發展趨勢與消費者需求，以軟性基板取代傳統硬式基板之電子產品便因應而生。晶片與軟性基板之接合大部份採用覆晶接合製程，但此一製程須精準控制膠之固化溫度與固化時間，顯見需控制之製程參數遠多於熱音波銲線接合，且熱音波銲線製程具有低成本與周邊基礎設備(infrastructure)發展完善等優點，然而熱音波銲線製程技術大多應用於硬性基板(rigid substrate)之接合，熱音波銲線接合製程應於軟性基板之相關研究極為少數，主要原因為軟性基板之勁度(stiffness)較低，銲線接合時易吸收熱音波製程之超音波能量，使超音波能量無法順利傳遞至金球銲點與軟性基板之接合介面，且因軟性基板剛性(rigidity)不足，接合時易使電極(electrode)陷入軟性基板中，使銲點無法成功銲著於軟性基板上方[1-3]。

熱音波銲線製程時，若金球銲點接合於未鍍著強化層之軟性基板上，在銲接下壓力(bonding force)與超音波功率(ultrasonic power)同時作用下，因軟性基板之剛性不足，使電極陷入軟板中 [4]，易造成超音波能量無法完全傳遞至接合介面，影響熱音波銲線製程之銲著率與接合強度，故部分學者提出於軟性基板中，增加一層以高彈性模數為主之強化層，如鈦、鎳、鉻…等金屬薄膜，以防止軟板電極陷入軟性基板中[5]。Takeda等人[6]於研究中探討不同鍍膜層強化軟性基板剛性之可行性，改變聚乙醯胺(polyimide)軟性基板上銲墊(pad)鍍膜結構，研究結果指出，當銲墊僅有金鍍層時，採用30 g或40 g下壓力時，隨超音波功率之增加，銲墊之下陷量隨之增加，由此現象顯示大部份之超音波功率被軟性基板所吸收，造成銲墊之下陷，使金球銲點無法與銲墊產生接合；反之，若於銲墊鍍層上增加一層厚度為3 μm之鎳鍍層時，使用相同下壓力時，銲墊之下陷量不隨超音波功率之增加而提高，僅在一有限區間中變化，當銲墊之剛性提高後，大部份超音波功率可有效傳遞至接合介面，使其順利完成接合，並有效減少銲墊於熱音波銲線製程之下陷量(cupping)，當銲墊之下陷量減少，金球與銲墊之銲著率與接合強度隨之升高，亦即提高銲墊之剛性，應可有效提升超音波功率之傳遞。Heinen [7]與Murali [8]等人於聚乙醯胺軟性基板之銲墊上增加0.5μm之鈦(titanium)層或鎢(tungsten)層，研究結果指出採用相同熱音波製程參數組合時，未鍍著強化層之銲墊於熱音波銲線製程之銲著率與銲著強度，遠低於鍍著強化層之銲墊，由此得知，金球銲點與軟性基板之接合，可經由強化層提高銲墊之剛性，進而提高超音波功率傳遞至接合介面之效率，提高熱音波銲線製程之銲著率與接合強度。

本研究將於軟性基板中鍍著鎳層，希望藉以提升軟性基板的剛性，使金球銲點順利銲著於軟性基板上方，並探討鎳膜強化層在熱音波銲線製程中的強化機理。

四、實驗方法

本實所採用之軟性基板為聚乙醯胺與銅層所構成，為提高金球銲點與軟性基板之銲著率與銲著強度，於銅層上分別鍍著二種不同厚度之鎳膜，厚度分別為0.2μm與0.5μm，因銅層於熱音波接合時，暴露於大氣中，易於表面形成氧化膜，進而影響金球銲點與軟性基板銅電極之銲著率與銲著強度，因此參考過去之研究結果[9]，於鎳膜鍍層上方鍍著0.5 μm之銀膜作為接著層，該接著層目的在於提高金球銲點與軟性基板之接合。隨軟性基板鎳鍍層厚度之改變，驗證鎳鍍膜厚度是否有助於超音波功率於

熱音波接合製程之傳遞，進而提升金球銲點與軟性基板之銲著率與銲著強度。

金球銲點銲著於軟性基板後，以掃瞄式電子顯微鏡（SEM）觀察金球銲點之直徑，利用推球剪力測試(ball-shear test)檢測金球銲點與軟性基板之銲著強度，並參酌業界泛用JEDEC standards[10]之最小剪力強度，可得知金球銲點強度與軟性基板銅電極之接合強度是否符合業界之規範；於推球剪力測試後，利用歐傑電子儀(AES)分析軟性基板上所殘留之物質，用以判斷其破壞模式(fracture mode)。並觀察金球銲點與軟性基板接合介面之微結構，綜整金球銲點之介面微結構組織觀察、銲著強度測試、金球銲點尺寸觀察，建立熱音波銲線製程之適當參數組合，並探討鎳膜鍍著層厚度在熱音波接合過程中之強化機理。

金球銲點成功銲著於具鎳層之軟性基板後之試片進行高溫儲存（HTS）之可靠度試驗，儲存溫度為150℃，測試時間為400小時，每隔100小時取出一組試片，進行推球剪力測試、接合介面與推利測試後之破斷面觀察，並利用歐傑電子儀之線掃瞄(line scan)分析經高溫儲存後，金/銀/鎳/銅原子間之交互擴散，綜整歸納分析上述之實驗結果，建立金球銲點與具鎳膜鍍著層軟性基板之熱音波銲線製程接合機理。

五、結果與討論

5.1 鎳層對金球銲點之銲著率及銲著強度的影響

以熱音波銲線製程進行金球銲點與軟性基板銅電極之銲線接合實驗，金球銲點分別銲著於未具鎳層、鎳層厚度 0.2μm 與鎳層厚度 0.5μm三種不同鍍膜之軟性基板銅電極，銲線製程參數固定載台溫度為 180°C、銲接時間 40 ms、銲接負荷 0.5 N，改變超音波功率由 5 units 至 75 units。金球銲點與軟性基板銅電極具不同鎳膜厚度之銲著率，如圖一所示，當超音波功率為 5 units 時，金球銲點無法成功銲著於無鎳層與具鎳層厚度 0.2μm 之軟性基板銅電極，推測原因為超音波功率太小，且二種軟性基板之剛性不佳，接合過程中大部份超音波功率被軟性基板所吸收，無法有效傳遞至接合介面，使金球銲點無法成功銲著於軟性基板，僅於軟性基板表面留下金球銲點摩擦痕跡，如圖二(a)所示；相同超音波功率下，金球銲點銲著於鎳層厚度 0.5μm之軟性基板銅電極時，因銅電極具較厚之鎳層，使大部份之金球銲點得以銲著於軟性基板銅電極，該銲著率約為 70%；當超音波功率提升至 50units 時，金球銲點銲著於軟性基板銅電極具鎳層厚度 0.5μm，其銲著率可達 100%，金線與軟性基板之接合外觀如圖二(b)所示，而金球銲點與銅電極無鎳層與銅電極具鎳層厚度 0.2μm 之銲著率分別為 80%與 90%，兩者均無法達到 100%高銲著率之要求，顯見鍍著鎳膜於軟板銅電極，可有效提高金球銲點與軟性基板銅電極之銲著率。

推球剪力試驗通常用於檢測金球銲點與軟性基板之銲著強度是否符合封裝業界常用之 JEDEC 規範，推球剪力試驗所要求之最小接合強度與金球銲點之直徑成正比，因金球銲點直徑越大，與軟性基板電極之銲著面積隨之增大，故所需之最小推球剪力值亦隨之上升。圖三所示為改變超音波功率對金球銲點與三種不同鍍膜軟性基板銅電極接合強度之影響，金球銲點與軟性基板銅電極之接合強度均隨超音波功率增加而上升，以電子顯微鏡觀察金球銲點之直徑，配合推球試驗之剪力值，即可判斷接合強度是否符合 JEDEC 規範所要求之最小強度。當超音波功率為 5units 時，金球銲點無法成功銲著於無鎳層與鎳層厚度為 0.2μm 之軟性基板銅電極，故其銲著強度為 0；超音波功率提升至 25units 時，金球銲點與三種不同鍍膜軟性基板銅電極之銲著率皆無法達到 100%(如圖一所示)且銲著強度值偏低，無法符合規範與業界所需之高銲著率；若超音波功率提升至 50units 時，金球銲點與鎳層厚度為 0.5μm 軟性基板銅電極之銲著率可達 100%，配合金球銲點直徑檢測結果得知，金球銲點平均直徑約為 105μm，如圖四(a)所示；金球銲點與軟性基板銅電極之平均推球剪力強度為 68.5gf，參照 JEDEC 規範之最低平均推球剪力強度為 62gf，顯示金球銲點與鍍著厚度 0.5μm 軟性基板銅電極之接合強度高於 JEDEC 規範之最低平均接合強度；當輸入之超音波功率持續增大至 65units 與 75units 時，金球銲點與軟性基板銅電極之接合強度提升至 70 gf，但因超音波功率過大，使得金球銲點直徑大幅上升，金球銲點之平均直徑分別為 118μm 與 126μm，如圖四(b)與(c)所示，相對於 JEDEC 規範之最低接合強度值分別為 80gf 與 92gf，顯示在此超音波功率下，金球銲點與軟板銅電極之接合強度均無法符合 JEDEC 規範。金球銲點與軟板銅電極鍍著鎳膜厚度為 0.2μm 之接合強度較金球銲點與軟板未鍍著鎳膜之接合強度為高，但金球銲點與

兩者之接合強度均低於金球銲點與軟板銅電極鍍著 0.5μm 鎳膜之接合強度，且在相同超音波功率下，金球銲點直徑之差異不大，以相同方法分析金球銲點直徑與接合強度關係，兩者均無法符合 JEDEC 規範之要求，此實驗結果證實於適當超音波功率(50units)與軟性基板銅電極鍍著適當鎳層厚度(0.5μm)可有效提升金球銲點與軟板銅電極之銲著強度，並符合業界相關規範之要求。

金球銲點銲著於軟板銅電極後，經金相研磨、拋光等試片製作程序，以電子顯微鏡觀察金球銲點與軟板銅電極接合介面之完整性，圖五(a)為金球銲點與無鎳鍍軟板層銅電極之接合介面，於較大倍率時，可清楚發現金球銲點與軟板銅電極間存在間隙(gap)，如圖五(b)所示，顯示金球銲點與軟板銅電極並未完全接著，此一觀察結果可說明金球銲點與軟板無鎳膜鍍層銅電極接合強度不佳原因，如圖三所示。圖六(a)為金球銲點接著於軟板銅電極具鎳膜鍍層，厚度為 0.5μm，金球銲點與軟板銅電極接著良好，於較高倍率下，並無發現任何間隙或脫層(delamination)等缺陷存在，如圖六(b)所示，此一介面觀察結果與圖三所示之接合強度值相符，此一實驗結果再次驗證，鍍著 0.5μm 鎳膜於軟板銅電極，確實有助於金球銲點與軟板銅電極之接合。

5.2 破斷面分析

5.2.1 EDS分析

金球銲點與無鎳膜鍍層之軟板銅電極接合後，經推球剪力測試，以電子顯微鏡觀察其破斷面型態，有助於判斷金球銲點與軟銅電極之破斷模式(fracture mode)，如圖七(a)所示，軟板銅電極上方有少量殘留物，因此以能量光譜儀(EDS)對銅電極上殘留物進行分析，圖七(b)為軟板銅電極上殘留物之 EDS 分析圖譜，顯示銅電極上少許之殘留物為金，金球銲點與軟板銅電極之主要破壞模式為 JEDEC 規範所述第一類(type 1)破壞模式[10]，推球試驗時，金球銲點於軟板銅電極上剝離(peel-off)，僅少量金球銲點殘留於軟板銅電極上方，該破壞模式與少量殘金於軟板銅電極，顯示金球銲點與無鎳膜鍍層軟板銅電極之接合強度不佳，該實驗結果與圖三所示之推球試驗相符。金球銲點接著於軟板銅電極具 0.5μm 鎳膜鍍層，經推球剪力測試後，其破斷面處疑似軟板銅電極之鍍膜被剝離，如圖八(a)所示，以 EDS 分析軟板銅電極破斷面之元素組成，其分析圖譜如圖八(b)所示，該破斷面之主要組成元素為銅，顯示銅電極上之銀/鎳鍍膜被剝離，故銅電極表面形成凹窩，該破壞模式為 JEDEC 規範之第六類(type 6)破壞模式[10]，該破壞模式為電極薄膜於推球剪力試驗時剝離，亦即銀/鎳鍍膜隨金球銲點剝離，金球銲點與銀膜接著層之接合強度遠高於銅電極中銅層與鎳鍍層之接著強度，且該推力強度高於 JEDEC 規範之最低要求，再次顯示鍍著適當厚度之鎳膜鍍層於軟板銅電極，有助提高金球銲點與軟板銅電極之接合強度。

5.2.2 歐傑電子成像分析

利用歐傑電子成像對無鎳層軟板銅電極之破斷面進行 Au 與 Cu 元素分析，圖九(a)為無鎳膜鍍層軟板銅電極之 SEM 二次電子影像圖，圖九(b)與圖九(c)分別 Au、Cu 元素之歐傑電子影像圖，由圖中之明亮程度可區分原子分佈濃度之高度，比對圖九(a)與圖九(b)，可清楚發現，少量殘留於軟板銅電極之元素為金；比對圖九(a)與圖九(c)，僅極少量之 Cu 元素分佈於軟板銅電極上，因金球銲點與軟板銅電極未產生良好接合，推球試驗時，金球銲點於軟板銅電極上剝離，並殘留少量金於銅電極上，而銅電極薄膜並為隨金球銲點剝離，故銅電極表面之主要元素為 Ag，僅熱音接合時，極少數之銀膜被剝離。以歐傑電子成像分析推球試驗後，軟板銅電極具 0.5μm 鎳膜鍍層之破斷面，分別進行 Au、Cu 與 Ni 元素分析，圖十(a)為推球試驗後，軟板銅電極之破斷表面二次電子影像圖，顯示推球試驗後，於軟板銅電極表面形成一凹洞，該凹洞之尺寸與金球銲點之直徑接近，顯示該凹洞為推球試驗後，銅電極鍍膜被剝離所形成之凹洞，圖十(b)、(c)、(d)分別為 Au、Cu 及 Ni 元素之歐傑電子影像圖，圖十(b)可知銅電極破斷表面並無金元素存在，圖十(c)顯示大量銅元素分佈於凹洞中，圖十(d)顯示少量鎳元素分佈於凹洞周圍，由此觀察結果得知，該凹洞表面之主要組成元素為銅，參照前述銅電極薄膜之結構可知銀膜接著層與鎳膜鍍層均隨金球銲點剝離，主要之破斷面發生於銅電極之鍍膜層，顯示金球銲點與銀膜接著層之強度高於銅電極鍍膜間之吸附力，此一結果亦可說明金球銲點與軟板銅電極具良好接合性。

由上述實驗結果得知，金球銲點與無鎳膜鍍層軟板銅電極之主要破斷面模式為金球銲點由接合介面剝離，其強度無法滿足 JEDEC 規範之要求；金球銲點與軟板銅電極具 0.5μm 鎳層之主要破斷面模式為金球銲點連同銀/鎳膜被剝離，銲著強度可達 JEDEC 規範所要求之最小接合強度。

5.3 金球銲點與軟性基板之銲著區域分析

金球銲點以熱音波銲線製程(超音波功率50units、銲接時間 40ms、銲接負荷 0.5N、載台溫度 180°C)接著於軟板銅電極後，以硝酸將銲著於銅電極之金球銲點以無外力的情況下自然分離，並以電子顯微鏡觀察金球銲點之接著痕跡。銲著於無鎳膜鍍層銅電極之金球銲點，其接合介面非常平滑，且無明顯摩擦痕跡，如圖十一(a)所示，而銲著於具 0.5μm 鎳膜鍍層銅電極之金球銲點，其接合介面出現粗造且明顯之摩擦軌跡，如圖圖十一(b)所示，推測金球銲點以熱音波能量銲著於軟板銅電極時，因超音波功率於接合介面所產生之摩擦所致。

由上述金球銲點之觀察結果得知，於相同熱音波銲線製程參數下，銲著於不同鍍膜結構銅電極之金球銲點，其接合介面的摩擦痕跡亦有明顯不同，合理推測金球銲點接著時，超音波功率有效傳遞至接合介面，接合介面所產生的摩擦痕跡也就越多。此一實驗結果間接印證銅電極之鎳鍍層有助於超音波功率之傳遞。

當熱音波銲線製程之載台溫度為室溫時，大部份金球銲點無法順利銲著於軟板銅電極，在軟板銅電極表面形成凹痕與摩擦軌跡，因此觀察軟板銅電極上未銲著金球銲點之痕跡，可推論熱音波銲線製程中，超音波功率之傳遞效率。當超音波功率為 50units 時，無鎳膜鍍層與具 0.5μm 鎳膜鍍層銅電極表面之摩擦軌跡有明顯不同，分別如圖十二(a)與圖十二(b)所示，無鎳膜鍍層銅電極之摩擦區域平均直徑為 47μm，而具 0.5μm 鎳膜鍍層銅電極之摩擦區域平均直徑可達 73μm，金球銲點與軟板銅電極之摩擦區域為熱音波銲線製程時，所導入超音波功率於金球銲點與軟板銅電極間產生摩擦所致，故較大之摩擦區域顯示於熱音波銲線製程時，超音波傳遞之金球銲點與軟板銅電極之超音波功率較大，且在相同製程參數下，金球銲點與具 0.5μm 鎳膜鍍層軟板銅電極之摩擦區域較大，顯示該介面之超音波功率較大，故推論鎳膜鍍層可有效提高熱音波銲線製程之超音波功率傳遞，若有較大超音波功率傳遞至金球銲點與軟板銅電極之接合介面，可有效提金球銲點與軟板銅電極之接合強度。

5.4 高溫儲存試驗

將金球銲點接著於具 0.5μm 鎳膜鍍層軟板銅電極之五組試片放入加熱爐中，進行高溫儲存之可靠度試驗，加熱溫度與持溫時間分別為 150°C 與 400 小時，首先於持溫 50 小時後，取出一組試片進行推球剪力試驗，持溫 100小時後，每隔 100 小時取出一組試片，進行相同之推球剪力試驗。實驗結果如圖十三所示，金球銲點與軟板銅電極之接著強度，隨持溫時間增長而提高，為進一步探討接著強度隨持溫時間增加而提高原因，以 Auger line scan 分析高溫儲存試驗 50 小時後，金球銲點與銅電極之接合介面，如圖十四(a)所示，金球銲點與軟板銅電極之接合相當完整，並無空孔或脫層等缺陷發生，該介面之觀察結果可輔助說明圖十三中接合強度無衰退之現象，銅層、鎳層、銀層與金球銲點間，其原子之交互擴散(atomic interdiffusion)如圖十四(b)所示。高溫儲存試驗 400 小時後，金球銲點與軟板銅電極之接合介面如圖十五(a)所示，接合介面無空孔與脫層等缺陷存在，顯示金球銲點與軟板銅電極具良好之接著，各鍍層間之原子交互擴散如圖十五(b)所示，經長時間及高溫環境的作用下，各層間擴散的情形明顯增加，由金/銀分佈交錯發現，金大量擴散至銀層，故金球與銀接著層之鍵結非常良好，銀/鎳分佈交錯處發現，銀接著層與鎳層亦產生良好的鍵結，鎳/銅分佈交錯處發現，銅層完全擴散至鎳層中，使銅層與鎳層產生良好的鍵結，且銅/鎳/銀/金層之間皆有產生交互擴散現象，故接合強度明顯上升，此結果與高溫儲存測試後之推球剪力試驗趨勢相符。

高溫儲存後，金球銲點與具鎳鍍層銅電極之接合強度隨持溫時間增長而上升，且介面上並未發現空孔或脫層等缺陷，故金球銲點與具鎳層銅電極之熱音波銲線製程應無高溫儲存可靠度之疑慮。

六、結論

由上述之實驗結果，可歸納以下結論：

1. 藉由鎳鍍膜層，熱音波銲線製程成功將金球接著於軟性基板銅電極，隨鎳膜厚度增加，金球銲點直徑、接合強度與銲著率均明顯上升，其中以具鎳膜鍍層厚度為 0.5μm之軟性基板銅電極最佳。
2. 藉由觀察金球銲點與軟性基板產生摩擦區域得知，接合面積隨鎳層厚度增加而上升，顯示鎳鍍膜層有助於超音功率傳遞至金球銲點與軟板銅電極之接合介面，進而提高其接合強度。
3. 高溫儲存測試後，金球銲點與軟性基板之銲著強度隨持溫時間的上升而提升，經由 Auger line scan 分析發現，金/銀/鎳/銅原子間相互擴散範圍有所提升，故使鍵結強

度相對增加。

4. 金球銲點與具 0.5μm 鎳鍍層軟板銅電極之熱音波適銲參數組合：超音波功率 50 units、接合負荷 0.5 N、接合溫度 180°C 與接合時間 40 ms。

七、計畫成果自評

本計畫已完成單一銲點與軟板銅電極之接合製程開發與接合機理之建立，對下年度金凸塊覆晶接合軟板具有相當重要之參考意義，目前研究成果投稿之會議論文如下，並於近日內綜整研究結果，投稿至 Microelectronic engineering 國際學術期刊：

1. 莊正利,范晃逢,敖仲寧,潘志軒,"以熱音波製程將金球銲點銲著於具鎳鍍著層之軟性基板研究", 中國機械工程學會第二十六屆全國學術研討會論文集,2009年
2. 莊正利,范晃逢,敖仲寧,潘志軒,"鎳鍍層提高軟板銅電極剛性之研究", 中國銲接年會,2009年
3. 莊正利,范晃逢,敖仲寧,陳輝達,"以鎳鍍層提高金線熱音波銲線製程於軟性基板銅電極之銲著率與銲著強度", 中國材料科學學會全國學術研討會論文集,2009年

八、參考文獻

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2. G. Heinen, R.J. Stierman, D. Edwards, L. Nye, "Wire Bonding Over Active Circuits", *44th Electronic Component and Technology Conf.*, May 1-4, 1994,Washington,D.C., p. 922
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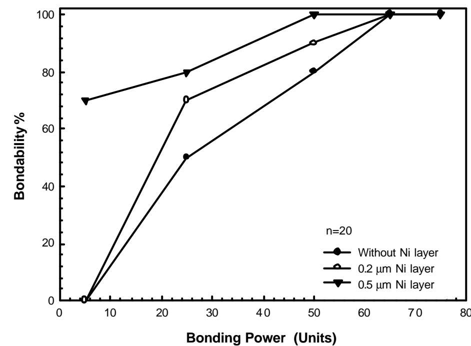
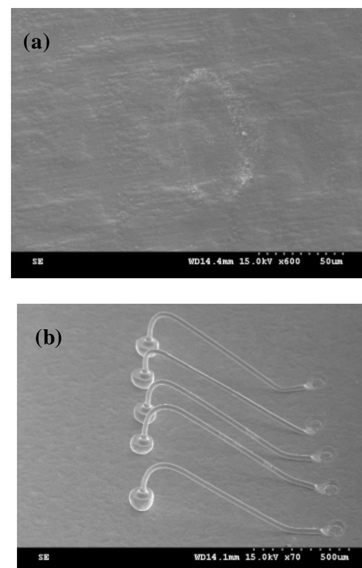
9. C. L. Chuang, J. N. Aoh," Thermosonic Bonding of Gold Wire onto Silver Bonding Layer on the bond pads of Chips with Copper Interconnects", Journal of Electronic Materials,2006, Vol.33, No.4, 290-299.
10. Joint Electron Device Engineering Council Standard 22-B116, "Wire Bond Shear Test Method",1998

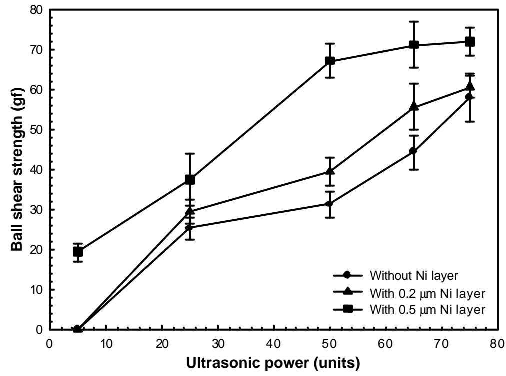
九、圖表



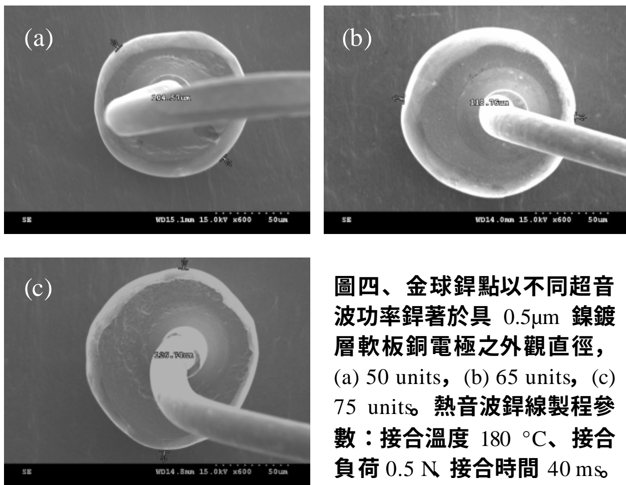
圖一、超音波功率對金球銲點與軟板銅電極之銲著率影響



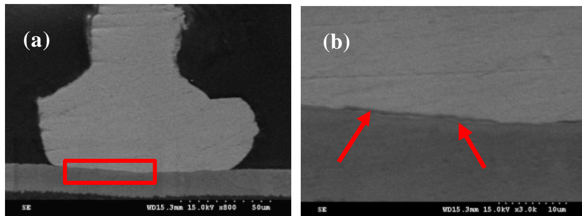
圖二、(a)超音功率 5units 時，金球銲點無法銲著於無鎳層銅電極之表面型態，(b)超音功率 50units 時，金球銲點成功銲著於鎳層厚度 0.5μm 銅電極之外觀圖



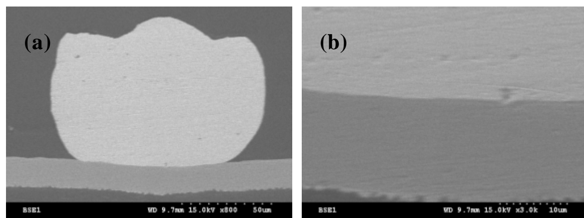
圖三、超音波功率對金球銲點與軟板銅電極之接合強度影響



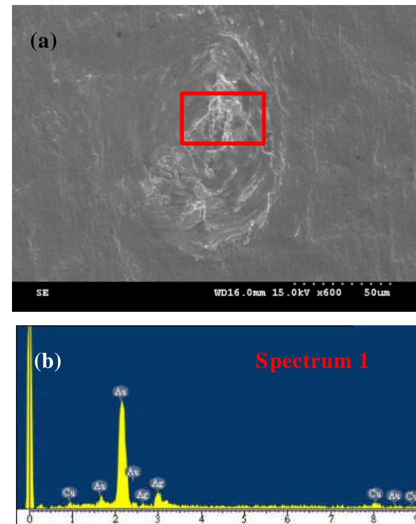
圖四、金球銲點以不同超音波功率銲著於具 0.5μm 鎳鍍層軟板銅電極之外觀直徑，(a) 50 units，(b) 65 units，(c) 75 units。熱音波銲線製程參數：接合溫度 180 °C、接合負荷 0.5 N、接合時間 40 ms。



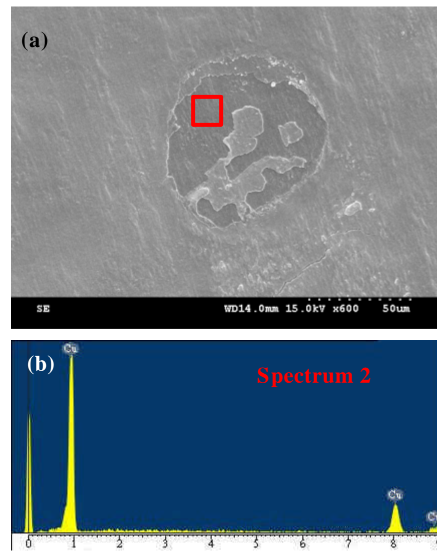
圖五、(a)金球銲點接著於無鎳層銅電極之橫截面，(b)金球銲點與無鎳層銅電極間存在間隙。



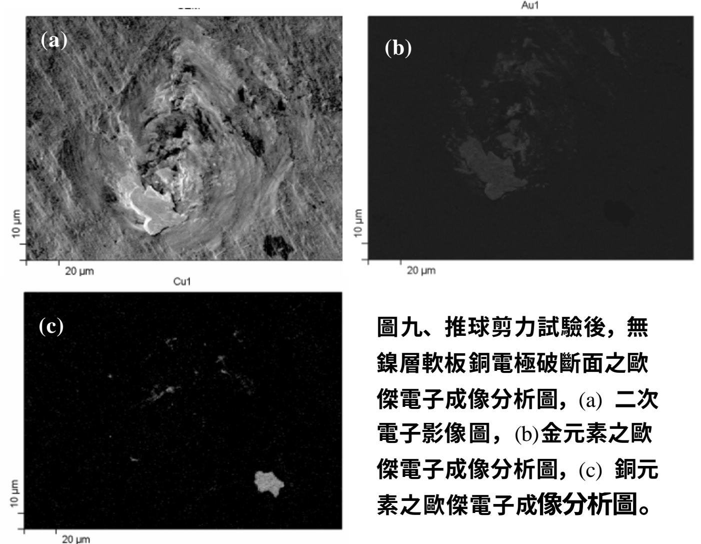
圖六、(a)金球銲點接著於鎳層厚度 0.5μm 銅電極之橫截面，(b)金球銲點與鎳層厚度 0.5μm 銅電極之接合介面無間隙



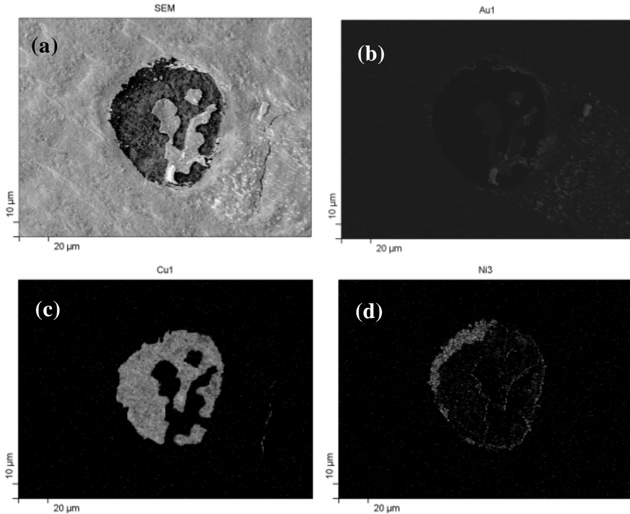
圖七、(a)推力試驗後金球銲點殘留於無鎳層銅電極之表面型態，(b)殘留銲點之能量散射光譜儀分析圖譜



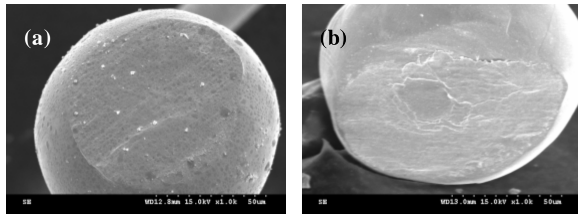
圖八、(a)推力試驗後具鎳層厚度 0.5μm 銅電極之表面型態，(b)破斷面之能量散射光譜儀分析圖譜



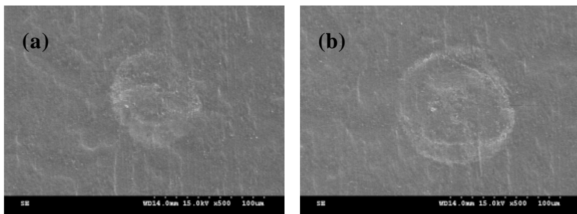
圖九、推球剪力試驗後，無鎳層軟板銅電極破斷面之歐傑電子成像分析圖，(a) 二次電子影像圖，(b)金元素之歐傑電子成像分析圖，(c) 銅元素之歐傑電子成像分析圖。



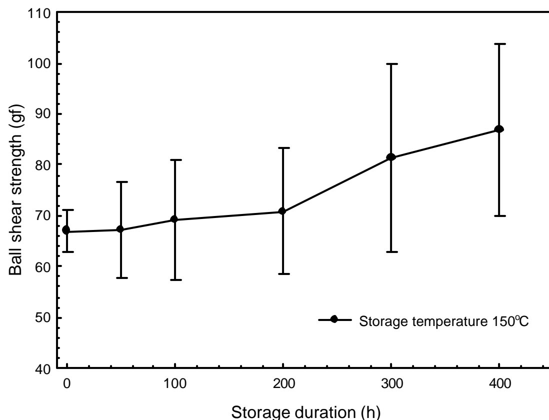
圖十、推球剪力試驗後，0.5μm 鎳層軟板銅電極破斷面之歐傑電子成像分析圖，(a)二次電子影像圖，(b)金元素之歐傑電子成像分析圖，(c)銅元素之歐傑電子成像分析圖，(d)鎳元素之歐傑電子成像分析圖。



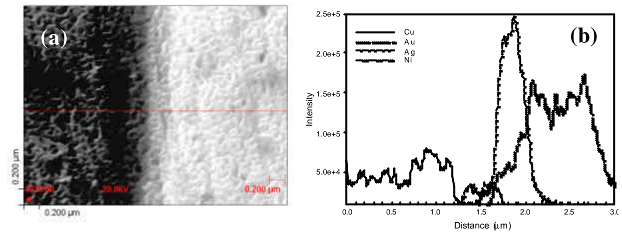
圖十一、(a)金球銲點接著於無鎳層銅電極後之銲點表面型態，(b)金球銲點接著於鎳層厚度 0.5μm 銅電極後之銲點表面型態



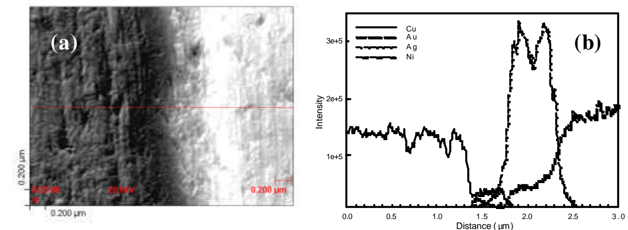
圖十二、金球銲點與銅電極未銲著區域，(a)無鎳層之軟性基板，(b)具鎳層厚度 0.5μm 之軟性基板（載台溫度：室溫，銲接負荷：0.5 N，銲接時間：40 ms，超音波功率：50units）



圖十三、高溫儲存時間對金球銲點與軟板銅電極接合強度之影響



圖十四、(a)高溫儲存 50 小時後金球銲點與具鎳層厚度 0.5μm 銅電極之接合介面，(b) AES 線掃瞄分析圖譜。



圖十五、(a)高溫儲存 400 小時後金球銲點與具鎳層厚度 0.5μm 銅電極之接合介面，(b) AES 線掃瞄分析圖譜。

96.6

出席國際學術會議心得報告

98 年 9 月 10 日

報告人姓名	莊正利	系所單位/職稱	中山醫學大學職業安全衛生學系 副教授
會議期間	Aug 10-13, 2009	會議地點	Beijing, China
主辦會議機構	China Semiconductor Industrial Association		
會議名稱	(中文)2009 微電子構裝與高密度封裝國際會議 (英文)2009 International Conference on Electronic Packaging Technology & High Density Packaging		
發表論文題目	(中文)矽晶片以非導電膠覆晶接合於軟板之可靠度研究 (英文)On Reliability of Chips bonded on Flex Substrates Using Thermosonic Flip-Chip Bonding Process with Nonconductive Paste		
所屬領域	工程		

報 告 內 容

一、參加會議經過：

本次微電子構裝國際學術會議係由大陸半導體協會主辦，並由北京清華大學微電子構裝研究所承辦，會議時間為 8 月 10 日至 13 日共 4 日，因微電子構裝技術在大陸蓬勃發展，故主辦單位在 8 月 8 日至 9 日舉辦微電子構裝技術之短期課程，內容涵蓋微電子構裝之發展趨勢、材料之應用、生產技術之提升與可靠度相關驗證等。今年會議主題可分為六大項：Advanced Packaging & System Integration、High Density Substrate & SMT:、Packaging Design and Modeling、Emerging Technologies、Packaging Equipment & Advanced Manufacturing Technologies、Quality & Reliability。**因大陸具有廣大消費市場，故各大微電子廠商紛紛前往大陸設廠，因此，在會議中不乏來自台灣的贊助廠商或構裝業者。本次會議參加人數上千人，四處可見各廠商之技術、研發人員穿梭於議場，尋找對其發展有利之生產技術，可見微電子構裝產業在大陸蓬勃發展，也可預見不久將來，對岸微電子構裝技術必然突飛猛進。**

二、與會心得：

主辦單位將議程第一天安排微電子構裝技術各領域專家進行專題演講，包括知名國際期刊 Microelectronic Reliability**主編** Michael Pecht **教授、日本東京大學** Tadastomo Suga **教授與** Rao Tummala **教授等，其中** Michael Pecht **教授提到目前消費性電子種類繁多，功**

能差異性大，發展趨勢為輕、薄、短、小，對元件或是系統之可靠度更是形成嚴重挑戰，並且業界泛用之 JEDEC Standards 也有超過 40 年，部分規範未隨發展技術之提升而修改，顯然無法符合目前微電子設備之發展需求，他也會議中，期勉所有參與微電子構裝技術發展的專業人士，能投入更多心力於可靠度之研究；而在構裝接合技術方面，來自日本 Suga 教授提出「自我活化接合(Self activated bonding ;SAB)」技術，從過去接合技術常用之熱壓接合(thermal compression bonding)、超音波接合(ultrasonic bonding)或熱音波接合(thermosonic bonding)轉換置凸塊(bump)與銲墊(bond pad)於常溫接合，演講中也展示日本 NHK 電視台對 Suga 教授研究項目之專題報導，而且該技術不僅用於微電子構裝領域，亦可使用傳統材料之接合，如鋁與銅因材料之熱傳導係數較高，故難以將兩種材料接合，Suga 教授用 SAB 製程已成功將鋁棒與銅棒接合，唯該製程需於真空環境完成，本人對此製程相當感興趣，故於演講結束後，私下請教 Suga 教授相關技術問題，他本人也相當程度公開該技術核心，同時也坦承該技術仍須再行研發與進步，因為製程穩定性不佳，製程可靠度需做進一步提升。

此次會議可發現目前大陸相關研究人員仍鎖定降低程度之銲線(wire bonding)封裝製程，特別是將金線轉換成銅線等降低生產成本研究，由此觀之，台灣在封裝相關技術上，仍保有一定程度的領先，但可見北京大學、清華大學研究生或專業教師熱烈參與封裝技術相關研究，可預期封裝技術在對岸官方、學界與業界大力支持發展下，將有爆炸性成長。

三、具體建議：

1.整體而言，該研討會算是相當成功，不僅國外專業人士投稿數量或品質，但會議流程與周邊配合事項，如會議用餐、人員管制與住宿旅館安排等，都有進步空間。

2.整個會議論文均提交登載於 IEEE 會議論文，若有國際知名學術期刊選擇品質較佳文章登載，應可提升參與發表論文品質。

3.參加國際會議除可培養國際觀外，更可與各領域傑出研究者討論，可提升研究能量，建議國科會應儘量補助研究人員參與國際學術會議。

五、攜回資料名稱及內容：

1.ICEPT-HDP 2009 PROCEEDINGS(ISBN:978-1-4244-4659-9)

2.SEMICONDUCTOR MANUFACRURING (ISSN:1555-9270)

3.EQUIPMENT FOR ELECTRONIC PRODUCTS MANUFACTURING (ISSN:1004-4507)

六、附件：

登載於 IEEE 資料庫之會議論文(如後所示)。

七、活動照片(具代表性之活動照片)：

編號 1. 攝於 2009 年 8 月 10 日，照片內容簡述：與會人員於北京清華大學主樓前團體照

編號 2. 攝於 2009 年 8 月 12 日，照片內容簡述：於會場外拍攝照片

編號 3. 攝於 2009 年 8 月 13 日，照片內容簡述：參觀北京清華大學圖書館

報告人簽章： 莊正利

On Reliability of Chips bonded on Flex Substrates Using Thermosonic Flip-Chip Bonding Process with Nonconductive Paste

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Abstract

The purpose of this study is to verify the reliability of chips bonded on flex substrates using thermosonic flip-chip bonding process with a non-conductive paste (NCP). High temperature storage (HTS) test, temperature cycling test (TCT), pressure cooker test (PCT) and high temperature/high humidity (HT/HH) test were conducted to investigate the reliability of chips bonded on flex substrates. The environmental parameters for reliability tests were complied with the JEDEC standards. After various reliability tests, the peeling test and microstructure observation on tested specimen were performed to evaluate the reliability.

The bonding strength increased with increasing the storage durations of HTS test. The HTS test provided sufficient thermal energy to promote atomic interdiffusion between Au bumps and Cu electrodes. A metallurgical bonding between Au bump and the Cu electrode was formed, and the bonding strength is thus improved. The bonding strength of chips and flex substrates assembly without applying ultrasonic in bonding process was decreased with increasing the storage durations of PCT. The typical failure for PCT was the interfacial delamination between NCP and flex substrates. Approximately 80% specimen exhibited fully separated after PCT at 336 h, implying the NCP cannot withstand the PCT test and lost its adhesion strength. The mean bonding strength of chips and flex substrates assembly with an ultrasonic power of 14.46 W in bonding process slightly varied with increasing storage durations of PCT, and standard deviation of bonding strength increased dramatically in the range of storage durations from 196 h to 336 h. Although the adhesion strength of NCP decreased, a part of Au bumps well bonded on Cu electrodes as the storage duration increased to 336 h. Applying the adequate ultrasonic power to bonding process was not only to improve the bonding strength, but also the bonding strength could be maintained in high level after PCT. There was no significantly change in bonding strength for chips bonded on flex substrates after TCT test. It shows that specimen has great reliability for TCT test. The bonding strength increased with increasing storage durations of HT/HH test. Neither cracks nor defects at boding interface are observed.

The reliability for chips bonded the flex substrate using thermosonic flip-chip bonding process with NCP meets the requirements stated in JEDEC specifications, exception of the adhesion strength of NCP for PCT should be improved.

Introduction

Adhesives have been widely used in microelectronics packaging for chips and substrates assembly [1-3]. The flip-chip bonding process with adhesives provides several advantages compared to conventional flip-chip bonding with solder bumps. It meets the environmental requirement, since the adhesive was lead free. There was no under-fill was required after flip-chip bonding with the adhesive, which is possible to reduce the manufacturing cost. The bonding strength of chips onto substrates was derived from the cured strength of adhesives. In our previous study [4], the thermosonic flip-chip bonding with NCP has been successfully applied to chips onto flex substrates. The ultrasonic power play an important role in scraping the NCP away from the surface of Cu electrodes, and then Au bumps directly bonded onto Cu electrodes to form a successful electrical path between chips and the substrates. With an appropriate value of ultrasonic power not only to scrape NCP away from the surface of Cu electrodes, but also provides a part of thermal energy to form the metallurgical bonding between Au bumps and Cu electrodes. Thus, this bonding technology is expected to offer several distinct advantages and enables achieving the low cost and excellent performance comparing with existed schemes.

Several studies investigated the reliability of chips onto substrates using adhesives [5-6]. Teh et al [5] verified the reliability of chips bonded on the rigid substrates using thermal compression bonding process with NCP. The experimental results indicated that NCP can easily pass the requirements of TCT and HTS test. However, most of specimen appeared interfacial delamination and opening between bumps and electrodes after reliability test of MST and PCT. Both MST and PCT failures were contributed to excessive stress generated due to moisture vaporization at high temperature. Similar experimental results were obtained for chips onto flex substrate using NCP after reliability tests [6]. The delamination appeared at interface between chips and the flex substrates after PCT. Up to now, no published literature was found to examine the reliability of chips and flex substrates assembly using thermosonic flip-chip bonding process with NCP.

The objective of this study is to verify the reliability of chips onto flex substrates using thermosonic flip-chip bonding with NCP. The HTS test, TCT, PCT and HT/HH test were conducted to investigate the reliability of chips bonded on flex substrates. The environmental parameters for reliability tests were complied with the JEDEC standards. After reliability tests, the peeling test and microstructure observation on tested specimen were performed to evaluate the reliability.

Experimental methods

A thermosetting type of commercial NCP was used in this study. The non-conductive paste was deposited on the surface of flex substrates, and a chip with eight Au bumps to be

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bonded onto Cu electrodes over the flex substrates using thermosonic flip-chip bonding process. The flip-chip bonding experiments were performed using an automatic thermosonic flip-chip bonder developed by the Industrial Technology Research Institute (ITRI). The deposited layers of bond pads and Cu electrodes were stated in our previous work [7]. To evaluate the effect of ultrasonic power on the reliability of chips bonded on flex substrates, two kinds of bonding process for chips and flex substrates assembly were performed in this study. The first bonding process is applied an ultrasonic power of 14.46 W to flip-chip bonding process with NCP for chips and flex substrates assembly. The other was no ultrasonic power applying in flip-chip bonding process to simulate the thermal compression bonding process with the NCP. Other bonding parameters are fixed at a bonding force of 10 N, a preheating temperature of 80°C, a curing temperature of 140°C and a cured time of 40 s.

After chips and flex substrates assembly, the specimen was subjected to various reliability tests, including HTS test, TCT, PCT and HT/HH test. The storage durations and tested parameters were complied with the JEDEC standards [8-11], as shown in Table 1. The peeling test was conducted to evaluate the bonding strength after the reliability tests.

Table 1 Lists of storage durations and environmental parameters for various reliability tests. [8-11]

	HTS	HT/HH	TCT	PCT
Test Conditions	+150 °C	+85°C/85% RH(no bias)	+125 °C /- 55 °C	+121 °C/ 100%RH 2atm
Read Point	200,400,600,800,1000 (hrs)	200,400,600,800,1000 (hrs)	100,300,500,800,1000 (cycles)	24,48,96,168,240,336 (hrs)
Test Duration	1000 hrs	1000 hours	1000 cycles	336 hs

Optical microscopy (OM) and scanning electron microscopy (SEM) were conducted to examine changes at bonding interface after various reliability tests. The fracture mode and the fracture mechanism after peeling test also verified using SEM and OM. Line scanning of the field-emission Auger electronic spectroscopy (FEAES) was used to determine the atomic inter-diffusion between Au bumps and Cu electrodes after reliability tests.

Results and discussion

The effects of ultrasonic power on the bonding quality

To identify the effects of the ultrasonic power on the bonding quality for chips and flex substrates assembly, the applied ultrasonic power to bonding process was set at 0 W and 14.46 W. And other bonding parameters were fixed, 10N in bonding force, 80°C in preheat temperature, 140°C in cured temperature and 40 s in cured time. Figure 1(a) shows an un-deformed Au stud bump and a layer of NCP existed in bonding interface between the Au bump and the Cu electrode when the applied ultrasonic power was zero. This is an inactive interconnect between Au bumps and Cu electrodes since the Au bump cannot be directly contact with the Cu electrode to form an electrical path. In contrast to Au bumps bonded onto Cu electrodes without applying ultrasonic power, the Au bump directly bonded on the Cu electrode to form a conductive path between chips and the flex substrates when the ultrasonic power of 14.46 W was applied to bonding process, as shown in Fig. 1(b). This experimental result indicates that NCP was scraped away from the surface of Cu electrodes by ultrasonic power during thermosonic flip-chip bonding process, and Au bumps thus bonded on Cu electrodes. An electrical path between chips and flex substrates can be achieved. Applied an adequate value of the ultrasonic power is an effective way to increase yields of the successful interconnects between chips and flex substrates.

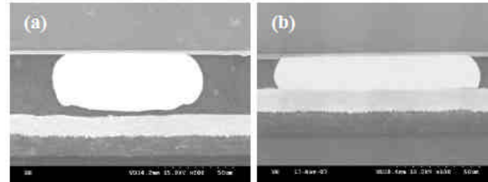

Fig. 1 SEM micrographs of (a) cross-section of chip bonded on the flex substrate without application of ultrasonic power, (b) cross-section of chip bonded on the flex substrate with an ultrasonic power of 14.46 W in flip-chip bonding process.

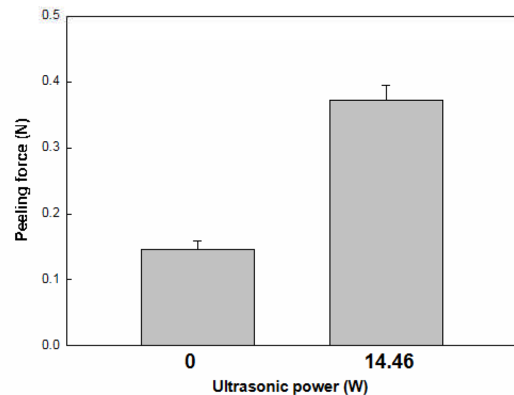

Fig. 2 The effect of ultrasonic power on the bonding strength of chips and flex substrates assembly.

The influence of the ultrasonic power on bonding strength of chips and flex substrates assembly was shown in Fig. 2. A higher bonding strength can be obtained when applied an ultrasonic power of 14.46 W to flip-chip bonding process with NCP than that flip-chip bonding without providing ultrasonic power. The increased bonding strength is assumed that was contributed to metallurgical bonding formation between Au bumps and Cu electrodes. After peeling test for chips and flex substrates assembly without applying ultrasonic power in bonding process, the fractured interface appeared a smooth surface without any scraping or any Au

bump residual, indicating fractured trace were propagated along between the NCP and Cu electrodes. Thus, the specimen of chips and flex substrates assembly without applying ultrasonic power in bonding process was designed to simulate the thermal compression bonding process with NCP. The peeling test after reliability test for this specimen was used to verify the adhesion strength of NCP.

High temperature storage test

Figure 3 displays the effect of storage durations on the bonding strength of chips and flex substrates assembly. No significantly change in bonding strength was observed for chips and flex substrates assembly without applying ultrasonic power in bonding process. The cured level of NCP was approximately 100% and no aging was found, the NCP thus maintained a steady adhesion strength for HTS test at storage durations varied form 0 h to 1000 h, indicating the NCP is able to withstand the HTS test. For chips and flex substrates assembly with an ultrasonic power of 14.46W, the bonding strength increases with increasing storage durations, revealing a good reliability. After HTS test at storage duration of 200 h, the fractured morphology of chips and flex substrates was shown in Fig. 4. A layer stuck on Au bump over the chip and a concavity was formed on the surface of flex substrates, as shown in Fig. 4(a) and 4(b). The dispersive spectrometer (EDS) was used to verify the composition of the layer stuck on Au bump. Figure 4(c) and 4(d) show morphology of the layer stuck on Au bump and the EDS spectrum, respectively. Only Cu peak was observed in the EDS spectrum, indicating that layer stuck on Au bump is Cu electrode. This analytical result indicates that the Cu layer was transferred to Au bump after peeling test. The bonding strength of Au bumps and Cu electrode are even higher than adhesion strength between Cu electrodes and polyimide substrate. A similar fractured morphology of chips and flex substrates was found after HTS test at storage duration of 1000 h. A sheet of Cu layer peeled off from the interface between Cu electrodes and the polyimide substrate, and the Cu layer transferred to the surface of chips (Fig. 5(a)), a concavity was thus formed on the fractured surface of flex substrates, as shown in Fig. 5(b). The observation on fractured morphology after peeling test consists with the changes of bonding strength at various storage durations, as shown in Fig. 3.

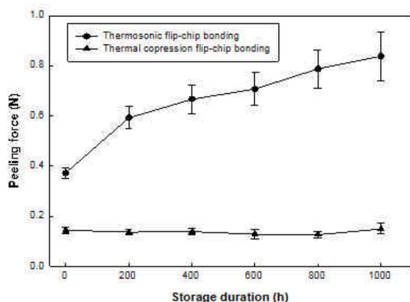

Fig.3 Relationships between bonding strength and storage durations of HTS for chips bonded on flex substrates heated at 150°C.

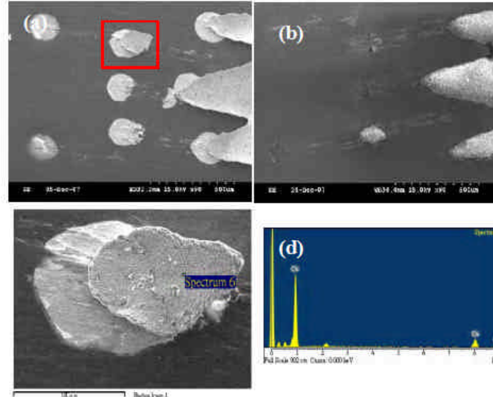

Fig. 4 SEM micrographs show (a) the fractured morphology of chips after peeling test, (b) the fractured morphology of flex substrates after peeling test, (c) a layer bonded on Au bump shown in (a) with a larger magnification, (d) the EDS analytical spectrum. The peeling test was performed after HTS test at storage

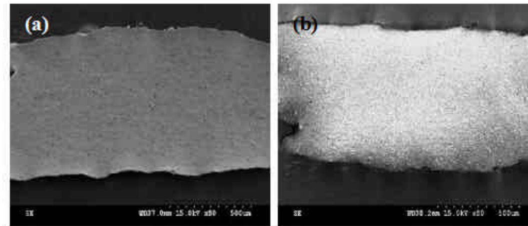

Fig. 5 SEM micrographs show (a) the fractured morphology of chips after peeling test, (b) the fractured morphology of flex substrates after peeling test. The peeling test was performed after HTS test at storage duration of 1000 h.

To investigate the possible change at bonding interface after HTS test for 200 h and 1000 h, the interface between Au bumps and Cu electrodes was examined using SEM. Neither delamination nor other defects were found at bonding interface as shown in Fig. 6(a) and Fig. 6 (b). A line scanning of FEAES was conducted to determine atomic interdiffusion between Au bump and the Cu electrode. A narrow atomic interdiffuion trace was observed at bonding interface for an as received specimen, as shown in Fig. 7. The atomic interdiffusion for an as received specimen could be attributed to thermal energy from cured process, 140°C for 5 s. In contrast to the narrow atomic interdiffusion trace for an as received specimen, the broadened atomic interdiffusion trace is observed after HTS test at 1000 h, as shown in Fig. 8. The atomic interdiffusion was promoted by the high temperature and storage durations, thus, resulted in increased bonding strength. This analytical result can be used to interpret the bonding strength increased with the storage durations of HTS test, as shown Fig. 3. Applying ultrasonic power to flip-chip

bonding process with NCP for chips and flex substrates assembly, not only the bonding strength was improved, but also the reliability of HTS test can be guaranteed.

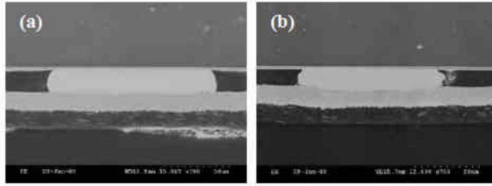

Fig. 6 SEM micrographs show (a) the cross section of Au bump bonded on the copper electrode after HTS test at storage duration of 200 h, (b) the cross section of Au bump bonded on the copper electrode after HTS test at storage duration of 1000

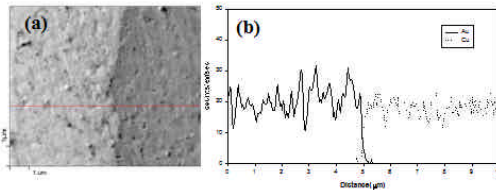

Fig. 7 Line scanning results on the cross section of Au bump and Cu electrode interface. (a) Cross section on interface between Au bump and Cu electrode, (b) atomic interdiffusion of Au bump and Cu electrode

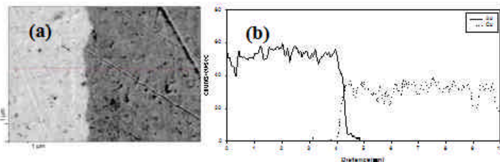

Fig. 8 Line scanning results on the cross section of Au bump and Cu electrode interface. (a) Cross section on interface between Au bump and Cu electrode after HTS test at storage duration of 1000 h, (b) atomic interdiffusion of Au bump and Cu electrode after HTS test at storage duration of 1000 h.

Temperature cycling test

The effect of TCT on the bonding strength of chips and flex substrates assembly was shown in Fig. 9. The variation of bonding strength for chips and flex substrates assembly without applying ultrasonic power in flip-chip bonding process after TCT at 1000 cycles is very small. The adhesion strength of NCP has a stable performance after TCT at 1000 cycles, which could be met the requirements stated in the JEDEC specifications. After TCT, the bonding strength of chip and flex substrates assembly with applying an ultrasonic of 14.46 W in flip-chip bonding process also varied in a narrow zone. To investigate the possible change in bonding interface after TCT at 100 cycles and 1000 cycles, the cross-section of Au bumps bonded on Cu electrodes was examined using SEM. As shown in Fig. 10, the Au bump firmly bonded on Cu electrode and no defects was found at bonding interface. This observation on bonding interface could be used to explain why bonding strength has a good reliability for TCT at 100 cycles and 1000 cycles, as shown in Fig. 9.

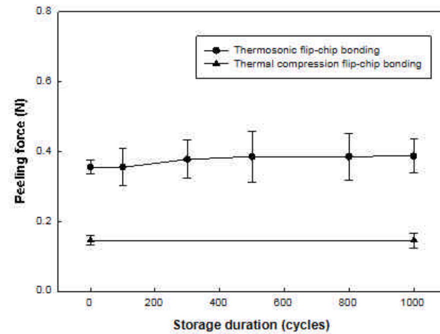

Fig. 9 Relationships between bonding strength and storage durations of TCT for chips bonded on flex substrates heated at 125°C/-55°C.

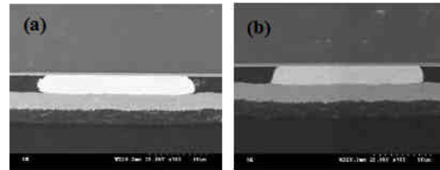

Fig. 10 SEM micrographs show (a) the cross section of Au bump bonded on the copper electrode after TCT at storage duration of 100 cycles, (b) the cross section of Au bump bonded on the copper electrode after TCT at storage duration of 1000 cycles.

Pressure cooker test

To investigate the reliability of chips and flex substrates assembly after PCT, the chips together with flex substrates were subjected to a highly humid (100% RH), a highly pressure (2 atm) and a highly temperature (150°C) for various storage durations. The influence of PCT on bonding strength of chips and flex substrates assembly is illustrated in Fig. 11. The bonding strength of chips and flex substrates assembly without applying ultrasonic in bonding process was decreased with increasing the storage durations. The typical failure for PCT was the interfacial delamination between NCP and flex substrates. Approximately 80% specimen exhibited fully separated after PCT at 336 h, as shown in Fig. 12. The adhesion strength of NCP was deteriorated after PCT. This phenomenon could be used to explain the bonding strength of chips and flex substrates assembly without applying ultrasonic power in bonding process decreased with

increasing storage durations of PCT. This experimental result also indicates that adhesion strength of NCP for PCT should be improved. The mean bonding strength of chips and flex substrates assembly with an ultrasonic power of 14.46 W in bonding process slightly varied with increasing storage durations of PCT, and standard deviation of bonding strength increased dramatically in the range of storage durations from 168 h to 336 h, as shown in Fig. 11. To find out the changes at bonding interface between chips and flex substrates, the SEM was used to examine the cross section of Au bumps bonded on Cu electrodes. The Au bump well bonded on the Cu electrode, no delamination or others defects were found at bonding interface after PCT for 24 h and 96 h. as shown in Fig. 13. The slightly decreased bonding strength in the range of storage duration from 24 h to 96 h could be contributed by the lost adhesion of NCP. As storage duration extended to 168 h, a delamination was found at bonding interface between NCP and the chip, as shown in Figs. 14(a) and 14(b). However, a sound bonding interface can be found at interface between Au bump and the Cu electrode, as shown Fig. 14(c). The delamination also was found at chip edge and a crack also appeared at bonding interface between Au bump and the Cu electrode when the storage duration of PCT was increased to 240 h, as shown in Figs. 15(a) and 15(b), respectively. Similar defects of delamination were also found at bonding interface of NCP/flex substrate and NCP/chip when storage time increased to 336 h, as shown in Figs. 16(a) and 16(b). Although the NCP lost its adhesion and delamination was found at bonding interface after PCT at storage duration of 336 h, a part of Au bumps well bonded on the Cu electrodes, as shown in Fig. 16(c). The bonding strength of chips bonded on flex substrates using thermosonic flip-chip bonding process with NCP were attributed to cured strength of NCP and the bonding strength of metallurgical bonding between Au bumps and Cu electrodes. As mentioned in the observation on the cross section of chips bonded on flex substrates, the adhesion of NCP decreased and the delamination were found at bonding interface of NCP/flex substrate and NCP/chip when storage durations of PCT were increased from 168 h to 336 h. However, a part of Au bumps well bonded on Cu electrodes as the storage duration increased to 336 h. The bonding strength after PCT at various storage durations was attributed by the interaction of the NCP lost its adhesion strength and the increased bonding strength for metallurgical bonding formed between Au bump and Cu electrode. Theses observations on the changes of bonding interface after PCT at various storage durations could be used to interpret the standard deviation of bonding strength dramatically increased with increasing the storage duration from 168 h to 336h, as shown in Fig. 11. Figure 17 shows the fractured morphology of the chips after PCT at various storage durations. The fractured morphology of the chip has a good shine after PCT at storage duration 24 h, as shown Fig. 17(a). With increasing the storage durations of PCT, the color of chips gradually transformed into dark, as shown in Figs. 17(b) and 17(c). The phenomenon indicates that NCP cannot withstand high moisture under high-pressure condition after PCT for extending storage durations, and delaminations were found at bonding interface of NCP/chip and NCP/flex substrate. The moisture penetrated to bonding interface between NCP and chip, which results in standard deviation increased after PCT at storage durations from 168 h to 336h, as shown in Fig. 11. These experimental results imply that applied adequate ultrasonic power to thermosonic flip-chip bonding process not only to improve the bonding strength of chips and flex substrates assembly, but also the bonding strength could be maintained in high level after PCT at various storage durations.

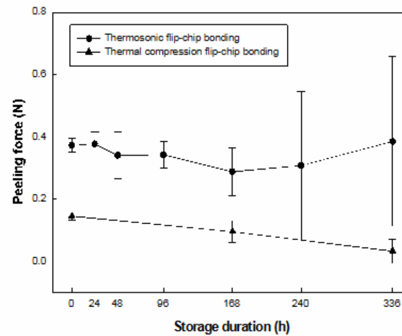

Fig. 11 Relationships between bonding strength and storage durations of PCT for chips bonded on flex substrates subjected at 121°C, 100% RH and 2 atm.

Fig. 12 The chips and flex substrates was fully separated after PCT at storage duration of 336 h. the chips and flex substrates assembly without applying ultrasonic power to flip-chip bonding process.

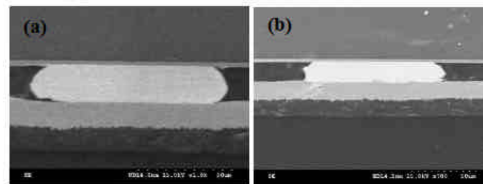

Fig. 13 SEM micrographs show (a) the cross section of Au bump bonded on the copper electrode after PCT at storage duration of 24 h, (b) the cross section of Au bump bonded on the copper electrode after PCT at storage duration of 96 h.

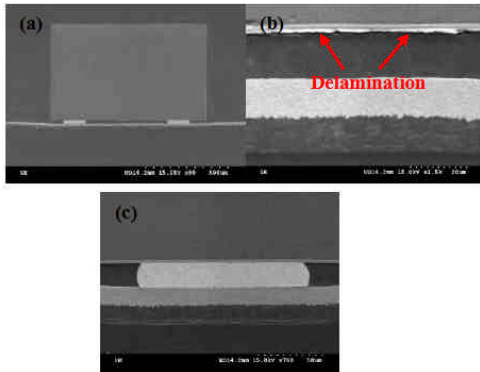

Fig. 14 SEM micrographs show (a) the cross section of chip bonded on flex substrate, (b) the delamination appeared at bonding interface between chip and NCP, (c) a Au bump well bonded on the Cu electrode without any defects

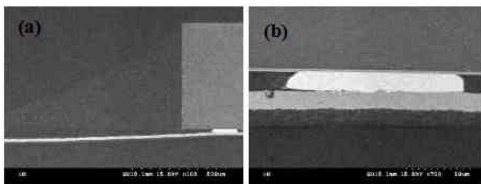

Fig. 15 SEM micrographs show (a) the delamination appeared at bonding interface between NCP and flex substrate, (b) the crack appeared at bonding interface between Au bump and Cu electrode. The specimen were subjected PCT at storage duration of 240 h.

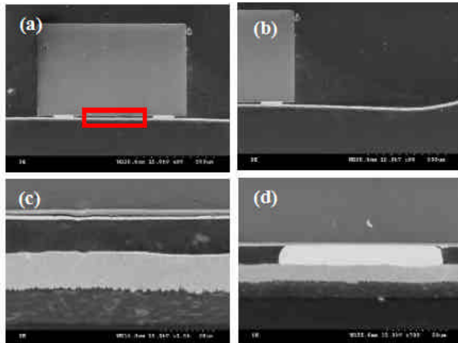

Fig. 16 SEM micrographs show (a) the cross section of chip bonded on flex substrate, (b) the delamination appeared at bonding interface between NCP and flex substrate, (c) the delamination appeared at bonding interface between NCP and chip, (d) a Au bump well bonded on Cu electrode without any defects. The specimen were subjected PCT at storage duration of 336 h.

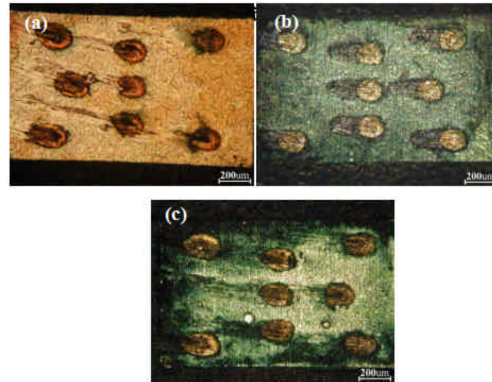

Fig. 17 Optical micrographs show the fractured morphology of chips after PCT at various storage durations, (a) 24 h, (b) 240 h, (c) 336 h.

High temperature/High humidity test

Figure 18 shows the relationship between bonding strength and storage durations of HH/HT test for chips bonded on flex substrates with and without applying ultrasonic power in flip-chip bonding process. For chips and flex substrates assembly without applying ultrasonic power, the bonding strength varied in a narrow range, indicates NCP with a good reliability after HH/HT test at various storage durations. As chips and flex substrates assembly with an ultrasonic power of 14.46 W, the bonding strength was increased with increasing storage durations of HH/HT test, as shown in Fig. 18. The cross-section of bonding interface between Au bumps and Cu electrodes were examined using SEM, no significant defects or cracks were found at bonding interface after HH/HT test at 200 h and 1000 h, as shown in Fig. 19. A clear interdiffusion trace between Au bump and Cu electrodes was obtained for chip bonded on flex substrates with an ultrasonic power of 14.46 W after HH/HT test at storage duration of 1000 h, as shown in Fig. 20. The bonding strength was improved by increasing the interdiffusion between Au bump and Cu electrodes. This experimental result can be used to explain that the higher bonding strength was obtained for chips and flex substrates assembly with the ultrasonic power after HH/HT test. In this study, the ultrasonic power is effective in improving bonding strength for chips bonded on flex substrates after HH/HT test. The reliability of HH/HT test for chips and flex substrates assembly using thermosonic flip-chip bonding process with NCP should not be a concern of issue.

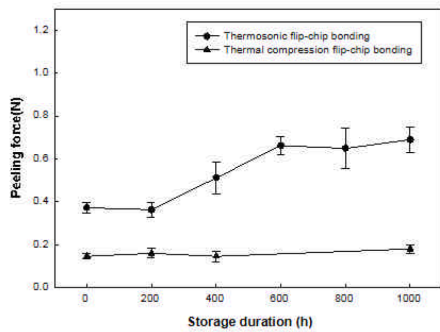

Fig. 18 Relationships between bonding strength and storage durations of HT/HH test for chips bonded on flex substrates subjected at 85°C, 85% RH.

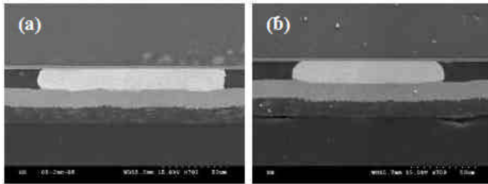

Fig. 19 SEM micrographs show (a) the cross section of Au bump bonded on the copper electrode after HH/HT test at storage duration of 200 h, (b) the cross section of Au bump bonded on the copper electrode after HH/HT test at storage duration of 1000h.

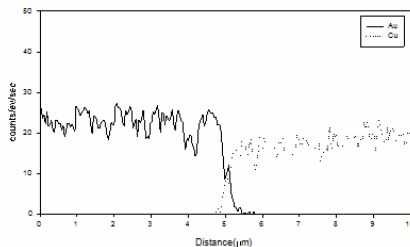

Fig. 20 Line scanning results on the cross section of Au bump and Cu electrode interface. The specimen was subjected to HH/HT test at storage time of 1000h.

Conclusions

The reliability of chips and flex substrates assembly using thermosonic flip-chip bonding process with the NCP has been verified in this work. For chips and flex substrates assembly without applying ultrasonic power, the NCP maintained a steady bonding strength after HTS test, TCT and HT/HH test, indicating that NCP has good reliability. Approximately 80% specimen, chips and flex substrates assembly without applying ultrasonic power in bonding process, exhibited fully separated after PCT at storage duration of 336 h. This observation implies that NCP cannot withstand the high pressure and high humidity testing condition, and lost its adhesion strength. Therefore, the adhesion strength of NCP should be improved for PCT. The bonding strength increased with increasing the storage durations of HTS test for chips and flex substrates assembly with the ultrasonic power of 14.46 W in flip-chip bonding process with NCP. As the HTS test provides sufficient driving force to promote the atomic interdiffusion between Au bumps and Cu electrodes, a metallurgical bonding was formed, and the bonding strength was thus increased. The mean values of bonding strength maintained in high level after PCT at various storage durations for chips and flex substrates assembly applying an ultrasonic power in bonding process. The standard deviation of bonding strength increased when the storage durations was extended from 168 h to 336 h. Delaminations were found at bonding interface of chip/NCP and NCP/flex substrate after PCT at storage durations from 168 h to 336 h. However, a part of Au bumps firmly bonded on Cu electrode after PCT at storage duration of 336 h. The standard deviation of bonding strength increased after PCT was attributed to interaction between the NCP lost its adhesion strength and the increased bonding strength for Au bump well bonded on the Cu electrode. Applying an adequate ultrasonic power in flip-chip bonding process can provide a high level bonding strength after PCT. There was no significantly change in bonding strength for Au bumps bonded on the flex substrates after TCT test. It shows the specimen has great reliability for TCT test. The bonding strength increased with increasing tested durations of HT/HH test. Neither cracks nor defects at boding interface are observed. The reliability of HT/HH test for chips bonded on flex substrates using thermosonic flip-chip process with NCP meets the requirements stated in JEDEC standards.

The reliability for Au bumps bonded the flex substrate using the thermosonic bonding process with NCP can meet the requirements stated in JEDEC specifications; exception of the adhesion strength of NCP for PCT should be improved.

Acknowledgments

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