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矽晶片以熱音波能量直接覆晶接合於軟性基板銅電極之製程開發與機理研究(III)
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矽晶片以熱音波能量直接覆晶接合於軟性基板銅電極之製程開發與機理研究(III)

The Reliability Investigation of chips and Flex Substrates Assembly Using Thermosonically Flip-Chip Bonding Process

一、中文摘要

本研究以熱音波製程將矽晶片接合於具鍍膜與無鎳膜之軟性基板，藉由軟性基板上之鎳膜提升晶片與軟性基板之接合強度，並施以高溫儲存、高溫蒸煮、溫度循環與恆溫/恆濕之可靠度加速試驗，實驗結果除評估金凸塊與軟性基板在不同加速試驗下之可靠度外，並探討其失效機制。

高溫儲存測試後，矽晶片與軟板之接合強度隨高溫儲存時間增加而些微降低，隨後在固定區間中變化。隨高溫儲存時間增長，晶片銲墊與金凸塊分離且金凸塊殘留於軟性基板上之斷面型態隨之增加，因矽晶片與金凸塊間熱膨脹係數之差異造成熱應力，導致金凸塊與矽晶片間產生脫層。由歐傑電子儀之分析結果顯示金凸塊與軟板銀膜接著層於高溫儲存後，金/銀原子間產生明顯之交互擴散。而晶片與軟板之剪力值並未明顯提升，其原因為熱應力與原子間交互擴散影響所致。

晶片與軟板接合之剪力值隨高溫蒸煮測試時間增長而大幅下降；剪力測試後之破斷面型態隨測試時間之增長，軟板銅電極鍍膜出現小半月形、大半月形、同心圓與接點內外鍍膜剝離之變化；金凸塊與軟板銅電極之接合截面之觀察結果，亦可清楚發現高溫蒸煮48小時後，金凸塊接點邊緣產生脫層，336小時後，金凸塊與軟基銅電極完全分離，甚至接點外圍鍍膜與銅層也分離，其破壞機制為高溫蒸煮測試之水氣由金凸塊外側朝其內部滲入，並使軟板銅電極鍍膜接著強度下降而產生脫層之缺陷，致使高溫蒸煮測試後，晶片與軟板之接合強度大幅下降。

矽晶片與軟板之剪力值於溫度循環測試週期400次後，出現明顯下降，隨後於400至1000週期呈現較小區間變化，但測試週期大於400期後，其剪力值小於JEDEC規範之要求。於剪力測試後破斷面之觀察，隨測試時間之增長，金凸塊與晶片銲墊產生剝離且金凸塊殘留於軟性基板上之斷面型態隨之增加，推論矽晶片與金凸塊間，因熱膨脹係數之差異造成熱應力，導致金凸塊與矽晶片銲墊間產生脫層之缺陷，並且由金凸塊與矽晶片出現剝離位置之數量統計，得知矽晶片外側接點較易出現該種斷裂模式，其原因為晶片外側於溫度循環過程中產生之變形量較大所致。

剪力值隨恆溫/恆濕測試時間增長而下降，剪力測試後之主要破斷模式為金凸塊由矽晶片銲墊鍍膜分離，觀察晶片端之破斷面，發現斷面附近之銲墊鍍膜層出現氣泡結構，推論於高溫/高濕度測試環境下，水氣滲入晶片銲墊之鍍膜層，鍍膜脫離矽晶片而形成氣泡狀之缺陷，若此氣泡產生於金凸塊與銲墊之接著區域，金凸塊與矽晶片銲墊之剪力值出現明顯下降。

綜觀高溫儲存、高壓蒸煮、溫度循環與恆溫/恆濕之可靠度實驗結果，以熱音波覆晶將矽晶片接合於具鎳鍍膜之軟性基板的製程可通過高溫儲存試驗，而高溫蒸煮測試之破壞機制為濕氣進入銅電極鍍膜中，造成鍍膜之剝離而破壞；矽晶片與軟性基板之剪力值隨溫度循環測試時間增長而下降之主因為金凸塊與矽晶片間因熱膨脹係數差異，繞應力於金凸塊與矽晶片經產生脫層缺陷所致，而恆溫/恆濕測試之失效主因為長時間高濕度引致水氣侵入矽晶片銲墊薄膜而出現氣泡缺陷所致。為確保晶片與軟板之接合可靠度，避免濕氣侵入金凸塊與銅電極之接合區域，確實有其必要性。

關鍵詞:熱音波覆晶接合、軟性基板、高溫儲存測試、高溫蒸煮測試、溫度循環測試、恆溫/恆濕測試。

二、英文摘要

This study assesses the reliability of the high-temperature storage (HTS) test, pressure-cooker test (PCT), temperature cycling test (TCT) and high temperature/ high humidity (HT/HH) test for an assembly of chips thermosonically bonded onto flex substrates. A nickel layer was deposited on the surface of copper electrodes over the flex substrates; this layer should enhance the bonding strength of the chips and flex substrates assembly. After chips

were bonded onto the flex substrates, specimens were utilized to assess the reliability of the HTS, PCT, TCT and (HT/HH) tests. Environmental parameters used in the reliability test were consistent with joint electron device engineering council (JEDEC) specifications. After the reliability test, the die-shear test was applied to examine changes to the die-shear forces. The microstructure of test specimens was analyzed to evaluate reliability and to identify possible failure mechanisms.

Die-shear force decreased slightly as HTS test duration increased. When the duration of the HTS test was increased, the percentage of gold bumps that peeled off of the surface of copper pads on the chip side increased, and delamination existed at the bonding interface between gold bumps and bond pads of silicon chips. This delamination was due to thermal stress generated during the HTS test, and degraded the die-shear force of the assembly of chips and flex substrates. A clear atomic interdiffusion of gold and sliver was obtained by Auger line scanning after the specimen was subjected to the HTS test at 150°C for 1000 h. Atomic interdiffusion effectively improves the bonding strength. However, die-shear forces decreased slightly as the duration of the HTS test increased, indicating that decreases in die-shear forces during the HTS test were dominated by delamination between gold bumps and the bond pads of silicon chips.

With the PCT, die-shear forces decreased significantly as test duration increased, and die-shear forces were lower than the minimum requirements in the JEDEC specifications for test durations of 96-336 h. Delamination existed at the interface between deposited layers of copper electrodes after specimens were subjected to the PCT for various durations, and the typical failure mode was deposited layers of copper electrodes being pulled out by gold bumps after the die-shear test. Fracture location was the Ni/Cu interface. This delamination was mainly due to the inability of the deposited layer to withstand the high moisture, high pressure, and high temperature of the test environment. Moisture penetrated into the deposited layers of copper electrodes, deposited layers lost their adhesion, and delamination propagated to the bonding area from outside of the bond area to the central bond area as test duration increased. The gold bumps finally separated fully from the surface of copper electrodes; thus, die-shear forces decreased significantly as the PCT duration decreased.

Die-shear forces were significantly decreased with increasing the tested periods of TCT from 0 to 400 cycles, and then die-shear forces varied in the narrow range of 545 gf and 535 gf for further increasing tested periods of 400 to 1000 cycles. The die-shear forces were slightly below the minimum required measure of 547 gf. Three categories of fracture modes can be found in the specimens subjected to TCT after die-shear test, gold bumps peeled-off from the surface of bond pads on silicon chips, the deposited layer of copper electrodes was pulled-out by gold bumps and gold bumps peeled-off from the surface of copper electrodes. As increased the tested periods of PCT, gold bumps peeled-off from the bonds of silicon chips became a major fracture mode, and the dleamination existed at bonding interface between the gold bump and the bond pads of silicon chips. This delamination was contributed to that thermal stress forming due to mismatch of the thermal expansion coefficient between the gold bump and the silicon chip.

A blister appeared on the surface of bond pads of silicon chips after the HT/HH test with various tested periods. The moister penetrated to deposited layers of bond pads and then results in forming the defect of the blister. The major fracture mode was gold bumps pulled-out the deposited layers of bond pad after HT/HH test. The die-shear forces would depend on the location of blister formation after HT/HH test. A die-shear force would decrease if the blister formed at bonding area between the gold bump and the deposited layers of bond pads. Thus, an obvious fluctuation of die-shear forces was observed after specimens subjected the HT/HH test with various tested periods.

三、文獻回顧

隨著高科技產業的發展日新月異，使得電子產品所用的元件朝向輕、薄、短小及高功能性之高精密技術發展，促使產品尺寸微小化及方便攜帶。晶片與軟性基板接合技術，大部分採用膠合製程之覆晶接合技術居多，但此一製程須精準控制膠之固化溫度與固化時間[1-2]，顯見需控制之製程參數遠較熱音波直接接合為多，而熱音波覆晶接合於軟性基板，因軟性基板具撓性，超音波功率不易傳遞至接合介面，但如鍍著一層鎳膜將有助於超音波功率傳遞至接合介面，以提升接合強度與接著率[3-5]。Ji[6]等人以超音波銲線製程，將金線銲著於鋁銲墊上，經過高溫儲存後發現，金線與鋁銲墊間生成介金屬化合物(IMC)，因金線與鋁銲墊之擴散速率差異，介金屬化合物生成同時，易產生成柯爾達孔洞(Kirkendall voids)，此孔洞隨高溫儲存的時間增長而增加，最終孔洞聚合而成裂痕。Breach[7]等人探討金線與鋁銲墊於高溫儲存測試中之失效機制，於高溫儲存 1500 小時後，剪力測試明顯下降，於金相

橫截面發現金凸塊與銲墊間形成 Au₄Al，儲存時間至 2000 小時後部分 Au_4Al 氧化形成氧化鋁並析出金，接合界面形成氧化物同時，發現於接合界面有孔洞與裂縫生成，由於新生成之氧化鋁與金與金凸塊間接合強度不佳，且於接合界面有些許孔洞與裂痕，因而剪力明顯下降。Uno[8]探討銅線與鍍鈀之銅線，以熱音波銲線製程接合於鋁墊上，於高溫蒸煮試驗中，鍍鈀之銅線其可靠度較佳，經高溫蒸煮 400 小時後，觀察兩試片之接合界面，於鍍鈀之銅線與鋁墊接合界面，生成一層 0.2μm 厚的介金屬化合物，反觀銅線與鋁墊間有明顯的裂縫生成，鈀於高溫蒸煮測試中，作為擴散阻隔層阻止銅與鋁互相擴散形成介金屬化合物。Chuang[9]等人探討非導電膠結合熱音波覆晶接合製程，將矽晶片接合於軟性基板之可靠度研究，於高溫儲存測試中，金凸塊與軟板銲墊互相擴散，經剝離測試其強度略微上升，於高溫蒸煮測試中水氣入侵膠體，非導電膠與晶片間出現脫層，致使水氣入侵元件內部，致使晶片與軟板之接合強度大幅下降。

四、實驗方法

本實驗擬藉由熱音波覆晶接合製程將已植金凸塊之矽晶片直接接合於具鎳鍍膜與無鎳鍍膜軟性基板上，並施以高溫儲存、高溫蒸煮、溫度循環與恆濕/恆溫之可靠度試驗，測試條件如表一所示[10-13]，除探討以熱音波覆晶製程接合矽晶片與軟性基板於高溫儲存及高溫蒸煮之可靠度外，並進一步探討接合試片之失效機制。

矽晶片之銲墊鍍膜由內至外分別為：矽(Si)/鈦(Ti)/銅(Cu)/鈦(Ti)/銀(Ag)，鍍著鈦膜於矽晶片之目的為提高矽晶片與金屬鍍層之接著力(adhesive)，而介於銅膜與銀層之鈦膜則為擴散阻隔層(diffusion barrier layer)，防止植金凸塊時，銅原子擴散至銀層表面，隨後形成銅之氧化層，進而影響植金凸塊之強度，銲墊表面之銀膜則做為接著層(bonding layer)，期望提升植金凸塊之接合強度。軟性基板之結構為聚乙醯胺(PI)/銅(Cu)/鎳(Ni)/銀(Ag)，鍍著鎳膜之目的為提升軟板銅電極之剛性(rigidity)，進而於熱音覆晶製程中，有效將超音波功率傳遞至接合介面，提升金凸塊與軟板銅電極之接合強度(bonding strength)與接著率(bondability)。

各項可靠度測試後，矽晶片與軟板接合試片以剪力測試(die-shear test)檢驗金凸塊與軟性基板銅電極之接合強度變化；以掃描式電子顯微鏡(SEM)觀察及能量光譜儀(EDS)分析各項可靠度試驗後試片在不同測試時間下，剪力測試後之斷面型態與接合介面之微結構(microstructure)，並以歐傑電子儀(Auger spectrometer)分析金凸塊與軟板銅電極接合介面原子間之交互擴散(innter-diffusion)。綜整上述實驗之分析結果，判斷金凸塊與軟版間在不同測試時間下，金凸塊與軟性基板銅電極接合之失效機制，並評估此製程在高溫儲存、高溫蒸煮、溫度循與恆濕/恆溫測試之可靠度。

五、結果與討論

5.1 高溫儲存測試

5.1.1 剪力測試

將植將凸塊之矽晶片以熱音波覆晶接合製程直接接著於具鎳膜與未鍍著鎳膜之軟性基板後，將兩種接合接試片置於高溫儲存爐中，進行高溫儲存測試，測試溫度與時間分別為 150℃ 與 1000 小時，每隔 200 小時取出一組試片，進行剪力測試。

圖一所示為晶片與軟板銅電極在不同測試時間下之剪力值，由圖中可清楚發現矽晶片與鍍著鎳膜軟板銅電極之強度均高於晶片與軟板銅電極未鍍著鎳者，顯示鍍著鎳膜於軟板銅電極有助提高金凸塊與軟板銅電極之接合強度，該原因為鎳膜可強化軟板銅電極之剛性，於熱音波覆晶接合製程中，將超音波能量傳遞至金凸塊與軟板銅電極之接合介面，進而提升其接合強度[5]。隨高溫儲存測試時間增長，矽晶片與鍍著鎳膜銅電極之剪力值微幅下降，該剪力值於 800-700 gf 區間中變化，對照 JESD22-B116A 規範[14]中，最小平均剪力值之要求為 547 gf。故矽晶片與銅電極鍍著鎳膜之平均剪力值均遠高於該規範之要求；矽晶片與銅電極未鍍著鎳膜軟板之剪力值均小於規範之要求，如圖一所示，顯示金凸塊與軟板銅電極之接合強度不佳，而且高溫儲存測試之時間增長，其剪力值之變動亦不大，推論金凸塊與軟性基板若於熱音波覆晶接合製程中，未能達成良好之接著，其接合強度無法藉由高溫儲存測試之熱能提高原子間之交互擴散，進而提高其接合強度。

5.1.2 接合介面分析

為進一步瞭解經高溫儲存測試，金凸塊與銅電極鍍鎳軟板之接合介面之變化，試片經高溫儲存測試 1000 小時後之橫截面如圖二(a)、(b)所示，於圖二(a)中發現軟板隨矽晶片金凸而形成明顯之變形，因軟板之剛性遠低於金凸塊或矽晶片且具良好撓性(flexible)，於長時間(1000 小時)且高溫(150℃)測試狀態下，可產生形變(deformation)，而較不易因熱應力(thermal stress)而產生之缺陷；圖二(b)所示為較大倍率下，金凸塊與軟板銅電極之接合介面並未出現脫層(delamination)或孔洞(pore)等缺陷，故高溫儲存測試後，金凸塊與銅電極鍍著鎳膜之軟板具仍保持良好之接合介面。

以較大倍率觀察未經高溫儲存測試、高溫儲存測試 400 小時後與 1000 小時後，金凸塊與矽晶片銲墊之接合介面分別如圖三(a)、(b)與(c)

所示，未經高溫儲存測試之金凸塊與矽晶片銲墊之接合介面完整，未發現脫層等缺陷，而經高溫儲存 400 與 1000 小時候，金凸塊與矽晶片銲墊間可清楚發現脫層之缺陷，但金凸塊與軟性基板之介面接合良好且未發現缺陷，推論此脫層缺陷之產生原因為矽晶片具較佳之剛性且銲墊鍍層材料與金凸塊存在熱膨脹係數之差異，故於長時間與高溫之測試環境中，矽晶片銲墊與金凸塊之接合介面易產生熱應力，進而於金凸塊與矽晶片銲墊接合周圍產生脫層之缺陷，該缺陷可能導致高溫儲存測試後，矽晶片與軟板剪力值微幅衰退之原因。

5.1.3 破斷面分析

觀察剪力測試後之破斷模式 (fracture mode)，可歸納出三種破壞模式出現於未經高儲存測試或經高溫儲存測試後之試片，分別為金凸塊連同軟板鍍膜拔離(pull-out)、金凸塊與軟板鍍膜間產生剝離(peel-off)、金凸塊與矽晶片銲墊間之剝離(peel-off)，如圖四所示。金凸塊連同銅電極鍍膜拔離之破壞模式顯示金凸塊與軟板銅電極之接合強度大於銅電極鍍膜之接著力，故於剪力測試時由銅電極鍍膜層間破裂，如圖四(a)所示；而金凸塊與銅電極表面剝離或金凸塊與矽晶片銲墊表面剝離之破壞模式，圖四(b)、(c)所示，均表示金凸塊與軟板銅電極或金凸塊與矽晶片銲墊表面之接著情況不佳或經高溫儲存測候其接合介面產生缺陷所致，此兩種破壞模式均可能引致矽晶片與軟板接合強度之下降。

比較未經高溫儲存測試與在不同高溫儲存測試時間下，剪力測試後，金凸塊與軟板銅電極破壞模式之變化，如圖五所示。未經高溫儲存測試之試片經剪力測試後，其主要之斷裂模式為金凸塊連同軟板鍍膜拔離與少量金凸塊於銅電極表面剝離之破裂模式，並未出現金凸塊與矽晶片銲墊剝離之破裂模式，圖六(a)所示為軟板銅電極於剪力測試時，部分鍍膜被拔離而形成凹洞之表面型態，且於破裂周圍出現微小裂縫(crack)，圖六(b)為剪力測試後金凸塊殘留於矽晶片之表面型態圖，以能量光譜儀(EDS)檢測軟板銅電極與金凸塊殘留於矽晶片之組成元素，點 1(point 1)之組成元素為銅，點 2(point 2)之組成元素為鎳與銀，此一分析結果說明銅電極之部分鎳膜與銀膜於剪力測時，轉移至金凸塊表面，於銅電極表面形成凹洞，該結果顯示金凸塊與軟板銅電極具良好之接著強度。

圖七為高溫儲存測試 1000 小時後，矽晶片與軟板經剪力測試後之破裂模式，圖七(a)、(b)為金凸塊連同軟板鍍膜拔離之破裂模式，相對圖六所示未經高溫儲存測試之破裂模式相似，在軟板側部分鍍膜被拔離而形成凹洞；圖七(c)、(d)為金凸塊與軟板銅電極鍍膜間之剝

離，該破裂模式僅在軟板側表面留下金凸塊接著痕跡，且無銅電極鍍膜被拔離，但剪力測試後殘留於矽晶片側之金凸塊產生明顯變形且軟板銅電極鍍膜產生裂縫，顯示該斷裂模式之接合強度雖低於鍍膜拔離之破裂模式，但其接合強度不致太低；圖七(e)、(f)為金凸塊與矽晶片銲墊間剝離(peel-off)之破裂模式，金凸塊殘留於軟板側，而矽晶片銲墊接著區中間部分出現銲墊鍍膜被拔離而形成凹洞，銲墊接著外圍區域則未出現鍍膜拔離現象，顯示金凸塊與銲墊接著區之外圍部份在未進行剪力測試時，已出現脫層之缺陷，而該脫層缺陷來自於高溫儲存測試時所形成之熱應力所致，此一結果與圖三金凸塊橫截之觀察結果相符。

隨高溫儲存測試時間增長，金凸塊連同銅電極鍍膜拔離之破裂模式便逐漸下降，而由金凸塊與軟板鍍膜間產生剝離、金凸塊與矽晶片銲墊間之剝離破裂模式隨之提高，如圖五所示。顯示於高溫儲存測試中，因矽晶片與金凸塊之熱膨脹係數差異，因而於接合介面產生熱應力，導致斷裂於晶片端之百分比增加，此一結果引致矽晶片與軟板接合強度之微幅下降，斷面觀察結果與高溫儲存測試後橫截面觀察結果(圖三)、剪力值之變化(圖一)相符。

5.1.4 接合介面之歐傑電子能譜儀分析

以歐傑電子能譜儀進行線掃瞄 (line scanning)分析接合介面間原子之交互擴散現象，圖八(a)為高溫儲存 1000 小時後，金凸塊與軟板銅電極之接合介面微結構 (microstructure)，圖中可清楚發現金凸塊與軟板銅電極具良好接著且無孔洞或脫層等缺陷，銅電極鍍膜與金凸塊間未發現介金屬化合物(intermetallic compound)之存在，圖八(b)為接合介面元素之線掃瞄結果，經高溫儲存 1000 小時後，金銀原子明顯產生交互擴散，少量金原子擴散至鎳層中，該金、銀原子之交互擴散有助於提升接合介面之接著力。

綜整上述之實驗結果得知，經高溫儲存測試後，金銀原子產生明顯交互擴散，應有助於接著強度之提升，但金凸塊與晶片銲墊間因熱膨脹係數差異所引致金凸塊於晶片端形成接合介面之脫層缺陷，隨高溫儲存時間之增長，由晶片端斷裂之模式增加，故高溫儲存測試後，矽晶片與軟板之剪力值較未進行高溫儲存測試者之剪力值微幅下降。

5.2高溫蒸煮測試

5.2.1剪力測試

矽晶片接合於軟板之試片經高溫蒸煮測試後，以剪力測試矽晶片與軟板剪力值之變化，矽晶片接合於具鎳鍍膜軟板之剪力值隨高溫蒸煮試驗時間增長而大幅下降，且於測試時間 96 小時候，該剪力值低於 JEDEC 規範最低

平均剪力值 547 gf 之要求，如圖九所示，後續擬觀察金凸塊與軟板接介面之顯微結構與剪力測試後之破斷模式，判斷該試片之可能原因與相關機制。而矽晶片與未鍍鎳膜軟板之接合強度亦隨高溫蒸煮測試時間增長而降低，但其下降幅度遠低於矽晶片接著於具鎳膜之軟板試片，推測其原因為矽晶片與為鍍鎳膜軟板之接合強度在未進行高溫蒸煮試驗時，其剪力值遠低於 JEDEC 規範之最低要求，顯示矽晶片與軟板之接合品質不佳，故後續進行高溫蒸煮試驗時，其下降幅度較為有限。

5.2.2 破斷面分析

矽晶片接合於鍍鎳軟性基板之試片經高壓蒸煮 24 小時後，剪力測試之破斷面如圖十(a)所示，該斷裂模式與未經過可靠度試片之破斷面相似，如圖六(a)所示，銅電極之鍍膜部分遭到拔離，鍍膜被拔離處呈半月形之凹窩，且於鍍膜拔離處周圍出現明顯裂痕；試片經過高壓蒸煮 48 小時，剪力測試後之破斷面如圖十(b)所示，銅電極鍍膜拔離面積已由半月形(圖十(a))擴展接近環狀之拔離，且被拔離鍍膜周圍並未發現裂痕，推測試片經高壓蒸煮 48 小時候，高壓蒸氣由金凸塊與軟板銅電極接合處周圍侵入，於金凸塊接合區域周圍產生銅電極鍍膜之脫層，剪力測試時該脫層之鍍膜轉移至金凸塊表面，該脫層之鍍膜可能造成矽晶片與軟板剪力值下降；圖十(c)為矽晶片與軟板接合試片經高壓蒸煮 96 小時，剪力測試後之破斷圖，銅電極鍍膜被拔離區域擴展成同心圓之斷裂模式，顯見高壓蒸煮之蒸氣侵入銅電極鍍膜層之影響更為明顯；分析經高壓蒸煮測試 336 小時，試片經剪力測試之破斷面如圖十(d)所示，軟板銅電極之鍍膜於剪力測試過程中，軟板上銅電極之鍍膜出現層狀之撕裂，推測高壓蒸氣完全滲入軟板銅電極鍍膜層中，造成軟板銅電極鍍膜接著之劣化，故於剪力測試時，軟板銅電極之鍍膜整層被拔離，該斷面觀察結果與剪力測試所得之剪力值趨勢相符(圖九)，推論矽晶片與軟板接合試片於高溫蒸煮試驗之破壞機制為高壓蒸煮之蒸汽由金凸塊與銅電極接合之鍍膜層滲入，隨測試時間之增長，侵入水氣隨之增多，造成銅電極鍍膜層間之脫層缺陷，致使矽晶片與軟板之接合強度大幅下降。

5.2.3 接合介面觀察

為進一步探討矽晶片與軟板接合試片於高壓蒸煮試驗之破壞機制，以電子顯微鏡(SEM)觀察經高壓蒸煮試驗後金凸塊與軟板銅電極接合之橫截面。經過高壓蒸煮測試 24 小時後，金凸塊周圍出現微細之脫層缺陷，如圖十一(a)所示；經高壓蒸煮測試 48 小時後，金凸塊與銅電極接合介面出現明顯之脫層缺陷，如圖十一(b)所示，隨高壓蒸煮測試時間之增長，金凸塊與銅電極完全分離，如圖十一(c)、(d)所示，金凸塊與軟板銅電極接合處之脫層缺陷隨高壓蒸煮測試時間增長而擴展至整個接合區域，此一橫截面觀察結果與剪力測試後，軟板銅電極表面之斷裂型態一致，驗證高壓蒸煮測試時蒸汽滲入銅電極鍍膜中，鍍膜間產生脫層之缺陷，致使整層鍍膜被拔離之破壞機制。

為檢測銅電極鍍膜於高壓蒸煮測試後，鍍膜脫層之發生處所，以能量光譜儀(EDS)檢視金凸塊與軟板產生脫層缺陷處之元素分佈，圖十二(a)為經高壓蒸煮測試 48 小時候，金凸塊與軟板銅電極之橫截面圖，於脫層缺陷之上下端分析其組成元素，脫層缺陷上端(point 1)之元素組成為金、鎳、銀，脫層缺陷下端(point 2)之組成元素為銅，分別如圖十二(b)、(c)所示，此一分析結果說明高壓蒸煮測試之脫層缺陷發生於鎳膜與銅層之間。

圖十三與表三為檢測高壓蒸煮測試 48 小時且經剪力測試後之斷面元素分析，結果顯示軟板銅電極鍍膜被拔離處之主要組成元素為銅(point 1)，未被拔離鍍膜表面之元素為銀(point 2)，而殘留於晶片端金凸塊表面之組成元素為鎳(pint 3)與金(pint 4)，顯示被拔離之鎳膜轉移至金凸塊表面，此一分析結果與前述橫截面之元素分析結果一致，該結果可再次證明前述金凸塊與軟板銅電極於高壓蒸煮測試之破壞機制。

由橫截面與剪力測試後所得之破斷面得知脫層缺陷係由金凸塊與軟板接合處周圍產生，進而往金凸塊與銅電極接合內部成長，致使金凸塊與軟板銅電極分離而失效，由此失效機制推論填充底膠(uderfill)防止高壓水氣之滲入或以製程改善銅膜與鎳膜於高壓蒸煮測試之接著力，應是有效提高矽晶片與軟板於高壓蒸煮可靠度之方法。

5.3 溫度循環測試

5.3.1 剪力測試

經溫度循環測試後，矽晶片接合於軟性基板之試片經剪力試驗所得之剪力如圖十四所示，矽晶片接合於鍍著鎳軟板試片之剪力值經溫度循環測試 400 週期後，其剪力值由 830 gf 降至 540 gf，隨後於測試 400 至 1000 週期，剪力值維持在狹小區間變化，比對 JEDEC 規範之最小剪力值約為 547 gf，顯示矽晶片與具鎳膜軟板試片經溫度循環測試 400 週期後，其剪力值已低於相關規範之要求。矽晶片與未鍍鎳軟板接合試片經溫度循環測試後，其剪力值亦隨剪力測試週期之增加而降低，但矽晶片與未鍍鎳軟板之接合強度下降幅度低於矽晶片與具鎳膜軟板之接合試片，推測其原因為未經

溫度循環測試之矽晶片與未鍍鎳膜軟板試片之接合強度遠低於 JEDEC 規範之最低要求，亦即接合試片內存在許多接合缺陷或接合品質不佳，故於溫度循環測試時，其剪力值下降幅度較低。

5.3.2 破斷面分析

矽晶片接合於具鎳膜軟性基板試片經溫度循環測試 1000 週期後，剪力測試後之斷裂模式(fracture mode)可為三類，分別為凸禿塊自銅電極鍍膜拔離(pull-out)、金凸塊與軟性基板接合介面之剝離(peel-off)與金凸塊由晶片端銲墊剝離(peel-off)，三種斷裂模式分別圖四(a)、(b)與(c)所示。

溫度循環測試 1000 週期後，軟板銅電極鍍膜被金凸塊拔離而形成銅電極之破斷面如圖十五(a)，圖十五(b)所示為從軟板銅電極鍍膜拔離而殘留於矽晶片側之金凸塊，由軟板之破斷型態圖可清楚發現銅電極之鍍膜於剪力測試時，部分鍍膜被拔離而留下凹窩且殘留裂縫於銅電極表面，而殘留於矽晶片端之金凸塊則出現剪力測試後之塑性變形 (plastic deformation)，此一破裂模式與未經溫度循環測試之破斷模式相似，如圖六(a)與(b)所示。為進一步確認軟板銅電極鍍膜被拔離鍍膜之成分(composition)，以能量光譜儀分析於軟板銅電極鍍膜剝離處(point 1)，顯示該凹窩之鍍膜為銅，如圖十五(c)所示，而殘留於晶片端之金凸塊(point 2)主要成分為鎳、磷與銀，如圖十五(d)所示，此一分析結果顯示銅電極鍍膜被拔離的薄膜轉移至金凸塊上方，而且拔離介面位於鎳膜與銅膜之接合介面，金凸塊與銀膜之接合強度甚至高於銅電極鍍膜間之接著力，而軟板銅電極未被拔離區域(point 3)之主要組成為金與銀，如圖十五(e)所示，此結果說明部分金凸塊殘留於軟板銅電極，顯示金凸塊與銀膜具良好接著強度，晶片側凸塊中間區域(point 4)之主要組成為金與銀，如圖十五(f)所示，銅電極表面之銀膜亦部分轉移至金凸塊，代表金凸塊中間部分與軟板銅電極接著。由破斷面組成元素之分析與觀察殘留金凸塊產生明顯塑性變形之結果，得知此種斷裂模式顯示金凸塊與軟性基板具良好之接合強度。

矽晶片接合於金凸塊經溫度循環測試 1000 週期且經剪力測試後，金凸塊由軟性基板銅電極鍍膜剝離之破斷面，如圖十六(a)與(b)所示，軟性基板之銅電極鍍膜並未剝離，接點邊緣也未發現裂痕，僅留下金凸塊與軟板銅電極之接著區域，且殘留於矽晶片端之凸塊未產生明顯之塑性變形。由能量光譜儀分析軟板銅

電極表面接合區域之中間部份(point 1)與接合區域之外側部分(point 2)，兩者之主要組成元素為銀，如圖十六(c)與(d)所示，顯示無任何金凸塊殘留於軟板銅電極表面。對殘留於矽晶片金凸塊之中間(point 3)與金凸塊外側(point 4)進行元素分析，前者之主要組成元素為銀，後者主要為銀與金，如圖十六(e)與(f)，由元素分析之結果顯示，金凸塊與銅電極之接合品質不佳，銅電極鍍膜無明顯拔離且凸塊亦無明顯之塑性變形，且僅部分銀膜轉移至金凸塊之外側區域，此種破斷模式顯示矽晶片與軟板之接合強度不佳。

試片經溫度循環測試 1000 週期後，金凸塊斷裂於晶片端銲墊而殘留於軟板之破斷面，如圖十七(a)與(b)所示。以能量光譜儀分析殘留於軟性基板端之金凸塊，金凸塊上中間部分(point 1)之主要組成為銀，如圖十七(c)所示，顯示金凸塊該區域係由晶片銲墊鍍膜銀層剝離；分析金凸塊周圍區域(point 2)之主要組成元素為金，如圖十七(d)所示，推論該區域未進行剪力測試時，金凸塊與矽晶銲墊存在脫層(delamination)之缺陷，故其外觀呈現平滑且剪力測試後未發現矽晶片銲墊鍍膜元素。矽晶片銲墊鍍膜剝離處(point 3)之主要組成元素為鈦，未剝離處(point 4)之主要組成元素為銀，如圖十七(e)與(f)所示。由元素分析與破斷表面型態之觀察，得知此類破斷形式稱生於矽晶片端鍍膜，矽晶片銲墊周圍並無裂痕產生，且金凸塊也未變形，由此推論矽晶片銲墊與金凸塊經可靠度測試後，其接合介面已產生脫層缺陷，故此類破斷模式顯示矽晶片與軟板之接合強度不佳。

為進一步說明斷裂模式與溫度循環週期之關係，統計所有溫度循環試驗試片金凸塊總數之破斷模式，如圖十八所示，當隨溫度循環週期增加，金凸塊於晶片端銲墊剝離和金凸塊與軟性基板接合介面剝離之斷裂模式百分比隨之增加，此兩種斷裂模式均顯示矽晶片與軟性基板之接合強度不佳。金凸塊於軟板銅電極拔離之斷裂模式隨溫度循環週期增加而降低，但於溫度循環 400 週期後，此種斷裂模式維持於 20-25%區間，此破斷模式之趨勢與剪力值之變化(圖十四)相符，且溫度循環 400 週期後，金凸塊於晶片銲墊剝離之斷裂模式約佔 50-60%，故推論此種破模式為剪力值下降之主因。

試片經溫度循環後，統計試片所有金凸塊斷裂模式之發生位置，將本實驗使用矽晶片之金凸塊分為外圍與中央兩的部分，屬外圍之金

凸塊編號 ABCD；晶片中間金凸塊之編號為 EFG，如圖十九所示。溫度循環測試後，晶片外圍金凸塊破裂模式之統計結果，如圖二十所示，隨溫度循環週期增加，矽晶片外圍金凸塊主要破裂模式由軟板銅電極鍍膜拔離轉換成金凸塊與矽晶片銲墊鍍膜剝離且該種破壞模式在溫度循環測試週期於 200-1000 間，均維持 85-90%間；反觀晶片中間金凸塊之主要破裂方式為金凸塊從銅電極鍍膜拔離，如圖二十一所示，經過溫度循環測試 200 次後，銅電極鍍膜拔離之斷裂模式佔 86%，溫度循環測試 1000 次後，銅電極鍍膜拔離之斷裂模式佔 56%，顯然矽晶片中央之接點隨溫度循環週期增加，矽晶片中間金凸塊受溫度循環測試之熱應力影響，使得斷裂於晶片側與金凸塊從軟板銅電極接合介面剝離之斷裂模式逐漸增加。

　　經溫度循環測試後，矽晶片外側金凸塊與軟板之破裂模式以金凸塊從矽晶片銲墊剝離為主，由圖十六之分析得知，該破壞模式顯示未進行剪力測試前，其接合介面存在脫層缺陷，推論該脫層缺陷由於矽晶片於溫度循環測試時，矽晶片外側變形量較大，導致晶片外圍金凸塊大部分斷裂於晶片端。

5.3.3 接合介面分析

　　矽晶片接合於軟性基板試片經溫度循環測試後，以電子顯微鏡觀察其接合介面之完整性。溫度循環測試 200 週期後，可發現金凸塊與矽晶片銲墊間存在脫層之缺陷，如圖二十二(a)所示，隨溫度循環測試週期達 1000，金凸塊與矽晶片完全分離，如圖二十二(b)所示，經過溫度循環測試之試片，易於晶片端產生脫層，甚至完全分離，因此斷裂於晶片端之斷裂模式逐漸增加，矽晶片與軟板之剪力值亦隨循環週期增加而降低。此一觀察結果亦可印證金凸塊由晶片端銲墊之斷裂模式為剪力測試前脫層缺陷已存在於金凸塊與矽晶片銲墊間，而脫層缺陷係由溫度循環熱應力所致。

　　進一步了解矽晶片上的金凸塊接點位置受到溫度循環測試週期之影響，觀察晶片外圍金凸塊與中間金凸塊之橫截面，經溫度循環測試 1000 週期後之矽晶片中央金凸塊之橫截面，如圖二十三(a)所示，金凸塊與矽晶片銲墊外側出現脫層缺陷，而矽晶片外側金凸塊與矽晶片銲墊完全分離，如圖二十三(b)所示，因金凸塊與矽晶片銲墊鍍膜熱膨脹係數差異，且矽晶片因剛性較佳，溫度循環測試週期間，不易隨金凸塊而變形，故金凸塊與矽晶片易產生較大之熱應力，而晶片外圍之變形量較大，故晶片外圍金凸塊更容易產生矽晶片銲墊剝離之破裂模式。

5.4 恆溫/恆濕測試

5.4.1 剪力測試

　　矽晶片接合於具鎳軟板之試片經恆溫/恆濕測試後，剪力測試所得之剪力值，如圖二十四所示，該剪力值經恆溫/恆濕測試 200 小時後，降至約 700 gf，隨後隨測試時間之增長 (400-1000 小時)，其剪力值在 530 gf 與 620 gf 間變化，若對照 JEDEC 規範之最低要求 547 gf，則部分剪力值低於該規範之要求；矽晶片與未鍍鎳軟板之試片經恆溫/恆濕測試後，所測得之剪力值在狹小區間變化，推論因矽晶片與未鍍鎳軟板之接合度不佳，故隨恆溫/恆濕測試時間之增長，其剪力值無大幅度之改變，而剪力值均低 JEDEC 規範之要求，故後續不將此一試片納入破裂機制之探討。

5.4.2 破斷面分析

　　試片經恆溫/恆濕測試 1000 小時且經剪力測試後之主要破裂方式為金凸塊由晶片銲墊拔離鍍膜而破壞，如圖二十五(a)所示，矽晶片銲墊鍍膜明顯隨金凸塊被拔離，金凸塊與銲墊之接著區域近似圓形，但其拔離鍍膜出現部分不規則之鍍膜剝離(圖二十五(a)圓圈部分)，進一步將破斷試片傾斜 30 度觀察後，發現矽晶片銲墊鍍膜出現許多氣泡狀之隆起，如圖二十五(b)所示，以較大倍率觀察矽晶片銲墊鍍膜剝離處之外圍，清楚發現該氣泡應為銲墊鍍膜隆起所致，如圖二十五(c)所示，而於矽晶片非接著區亦可觀察相同之氣泡，如圖二十五(d)所示，推論該氣泡之形成原因為恆溫/恆濕測試之水氣滲入矽晶片銲墊鍍膜中，於長時間加熱後，該滲入水氣將鍍膜撐開形成氣泡，若此氣泡發生於金凸塊接著區域，剪力測試後則形成不規則之拔離區域(圖二十五(a))，造成剪力值之下降，反之若氣泡形成於金凸塊與矽晶片銲墊鍍膜接著區之比例較低，剪力值衰退幅度亦隨之降低，此一結果可說明剪力值於恆溫/恆濕測試後變動之原因(圖二十四)。

5.4.3 接合介面分析

　　經恆/溫恆濕測試200小時後之橫截面，如圖二十六(a)所示，金凸塊與矽晶片之接合介面出現脫層之缺陷，以更高倍率觀察金凸塊與銲墊鍍膜層間存在脫層缺陷，如圖二十六 (b)，對照於金凸塊與矽晶片銲墊之破斷面(圖二十四)，金凸塊與矽晶片銲墊鍍膜幾乎被拔離，顯示於剪力測試前金凸塊與矽晶片銲墊間已存在脫層之缺陷，剪力測試時可輕易將金凸塊與銲墊鍍膜拔離而破裂，故矽晶片與軟板之剪力值不佳。恆溫/恆濕測試400小時後之橫截面，如圖二十六(c)所示，以更高倍率觀察鄰近金凸塊接著區域之鍍膜，可清楚發現銲墊鍍膜已脫離矽晶片表面而形成氣泡狀之隆起物，如圖二十六(d)所示，由橫截面之觀察得知無論是金凸塊接著區域或金凸塊接著區域外圍，銲墊

鍍膜均可能形成氣泡狀之脫層缺陷，而該缺陷為恆溫/恆濕測試下，水氣進入矽晶片鍍膜層所形成之缺陷，導致剪力測試時金凸塊接著於銲墊鍍膜全部拔離，甚至金凸塊接著附近之鍍膜亦可能遭拔離，而矽晶片與軟板之剪力值隨測試時間之變動，應受氣泡脫層缺陷出現於金凸塊與銲墊接著區數量多寡而影響，因而矽晶片與軟板之剪力值隨恆溫恆濕之測試時間而變動。

形成氣泡之脫層缺陷，該脫層缺陷為剪力值下降之主要因素。

綜整上述之實驗結果，降低金凸塊與矽晶片銲墊間之熱應力與防止濕氣進入金凸銅電極鍍膜、矽晶片銲墊鍍膜為確保矽晶片與軟板可靠度之有效方法。

六、結論

高溫儲存測試後矽晶片與軟板之剪力值出現微幅下降，隨高溫儲存測試時間之增長，金凸塊與矽晶片銲墊之剝離個數隨之增加，且於橫截面之觀察金凸塊與矽晶片銲墊出現明顯的脫層缺陷，該脫層缺陷為高溫儲存測試時，金凸塊與矽晶片銲墊間因熱膨脹係數差異產生熱應力所致。歐傑電子儀分析結果得知高溫儲測試存後，金凸塊與銅電極間明顯出現金、銀元素之交互擴散，但矽晶片與軟板之剪力值並未隨之提升，推論高溫儲存測試後，矽晶片與軟板之接合強度主要金凸塊與晶片銲墊間產生之脫層缺陷所主導。

經高壓蒸煮測試後，矽晶片與軟板之剪力值大幅下降，並低於業界相關規範之要求，矽晶片與軟板接合試片於高壓蒸煮之破壞機制為高壓蒸煮之蒸汽由金凸塊與銅電極接合之鍍膜層滲入，造成銅電極鍍膜間產生脫層之缺陷，隨測試時間之增長，侵入水氣隨之增多，造成金凸塊與軟板銅電極分離而失效，致使矽晶片與軟板之接合強度大幅下降，脫層之缺陷出現於銅電極鍍膜之銅膜與銀膜間，故由此失效機制推論填充底膠(uderfill)防止高壓水氣之滲入或以製程改善銅膜與鎳膜於高壓蒸煮測試之接著力，應是有效提高矽晶片與軟板於高壓蒸煮可靠度之方法。

溫度循環測試後，矽晶片與軟板之剪力值明顯下降，由破斷模式數量之統計，得知金凸塊與矽晶片銲墊產生剝離之破斷模式隨循環週期增加而提高，該種斷裂模式大量出現於矽晶片外側之金凸塊，且金凸塊與矽晶片銲墊出現完全分離之缺陷，反觀矽晶片中間部分之金凸塊大多接合良好則接著良好，因金凸塊與矽晶片於溫度循環測試時產生熱應力而產生金凸塊與矽晶片銲墊脫層之缺陷，且矽晶片外圍產生叫大變形，故外圍凸塊易出現與矽晶片銲墊完全分離之缺陷，該缺陷亦造成矽晶片與軟板剪力值之大幅衰退。

恆溫/恆濕測試後，矽晶片與軟板之剪力值於測試初期明顯下降，之後隨測試時間增長而產生高低之變動，觀察剪力測試後之主要斷裂模式為金凸塊從矽晶片銲墊鍍膜拔離且矽晶片鍍膜出現氣泡狀之脫層缺陷，該缺陷形成原因為恆溫/恆濕測試時，水氣進入銲墊鍍膜中，長時間加熱下使銲墊鍍膜失去接著強度而

七、計畫成果自評

本計畫已發表之相關論文：

1. 莊正利,敖仲寧,張連壁,康銘儀, "矽晶片以熱音波覆晶接合於軟性基板後經高溫儲存與高溫蒸煮測試之研究"，中國機械工程學會第二十八屆全國學術研討會,2011。
2. 莊正利,敖仲寧,張連壁,康銘儀, "矽晶片以熱音波覆晶製程接合於軟性基板後經溫度循環與恆溫/恆濕測試之研究"，中國機械工程學會第二十八屆全國學術研討會, 2011。
3. C.L. Chuang, M.Y. Kang," The Reliability of the HTS Test and PCT for Chips and Flex Substrates Assembly Using Thermosonically Flip-Chip Bonding Process", submitted to Microelectronic engineering, 2011.
4. C.L. Chuang, M.Y. Kang," On the Reliability of TCT and HT/HH Test for the Assembly of Chips and Flex Substrates Using Thermosonic Flip-Chip Bonding Process", submitted to Microelectronic engineering, 2011.

八、參考文獻

1. D. Wojciechowski, J. Vaneteren, E. Reese, H.W. Hagedorn, Microelectronics Reliability, Vol. 40, 2000, p 1215.
2. J.C. Jagt, IEEE Trans Comp, Packaging, Manuf Technol- Part A. Vol. 21, 1998, p 215.
3. C. L. Chuang, Q. A. Liao, H. T. Li, S. J. Liao, G. S. Huang, Microelectronic Engineering, 2010, Vol. 87, 624–630.
4. C. L. Chuang, J. N. Aoh, C. H. Pan, submitted to Microelectronic Engineering.
5. C. L. Chuang, H. F. Fan Microelectronic Engineering, 2011, Vol. 88, 3080–3086.
6. Ji, M. Li, C. Wang, H.S. Bang, H. S. Bang, Materials Science and Engineering, Vol. 447, 2007, 111-118.
7. C. D. Breach, F. Wulff, Microelectronics Reliability, Vol. 46, 2006, 2112-2121.
8. T. Uno, Microelectronics Reliability, Vol.51, 2011, 148-156.
9. C. L. Chuang, Wei-How Chen, Hsun-Tien Li, Hui-Ta Chen, Microelectronic Engineering, 2010, 87, 2146–2157.
10. JEDEC standard, JESD22-A-103-B, "High temperature storage life", 2001.
11. JEDEC standard, JESD22-A-102-C, "Pressure cooker testing", 2000.
12. JEDEC standard, JESD22-A-101-B, "Temperature humidity test", 1997.

13. JEDEC standard, JESD22-A-104-B, "Temperature cycling test", 2000.
14. JEDEC (EIA) Solid State Technology Product Engineering Council (Arlington, 1998)
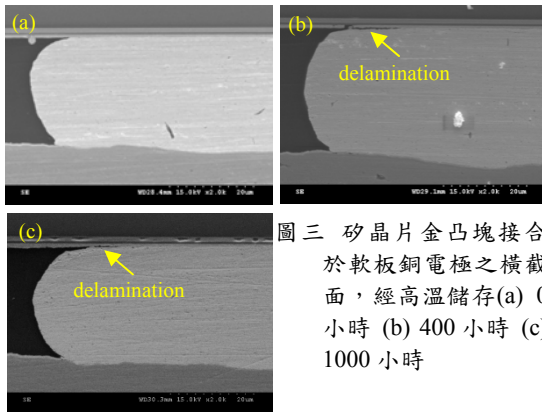
九、圖表

表一 可靠度測試條件[10-13]

	高溫儲存	溫度循環	高溫蒸煮	恆溫恆濕
測試條件	溫度：150ºC	溫度：-55ºC/125ºC 駐留時間：5min 升溫速率：15ºC/min	溫度：+121ºC 壓力：2atm 相對濕度：100%	溫度：+85ºC 相對濕度：85%
檢驗點	200,400,600,800,1000 hours	200,400,600,800,1000 cycle	24,48,96,168,240,336 hours	200,400,600,800,1000 hours
測試時間	1000 hours	1000 cycles	336 hours	1000 hours
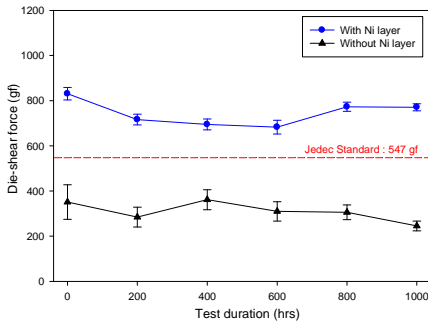
圖一 高溫儲存測試時間對剪力值之影響
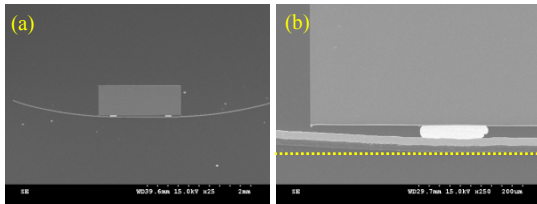
圖二 經高溫儲存 1000 小時 (a)矽晶片接合於軟性基板縱截面 (b)左側接點放大圖

圖三 矽晶片金凸塊接合於軟板銅電極之橫截面，經高溫儲存(a) 0 小時 (b) 400 小時 (c) 1000 小時
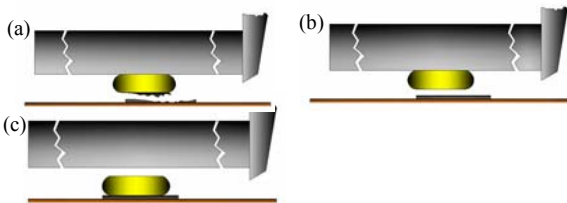
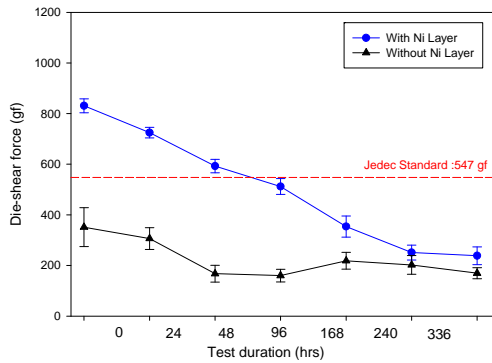圖四 剪力測試之斷裂模式 (a)銅電極銲墊鍍膜拔離 (b)金凸塊與軟板接合介面剝離 (c)金凸塊與晶片端銲墊之剝離
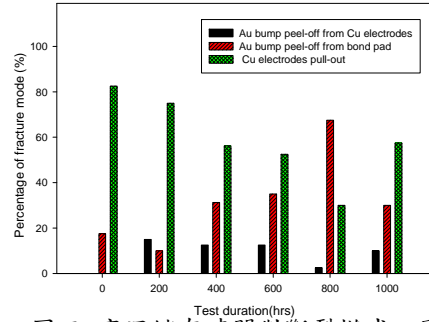
圖五 高溫儲存時間對斷裂模式之影響
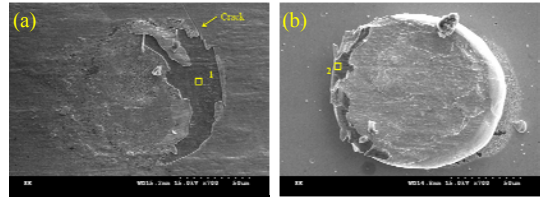
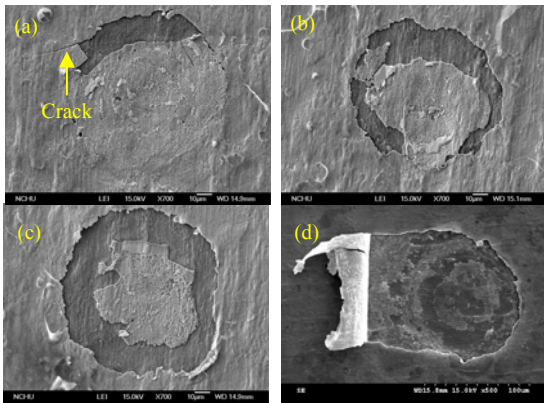圖六 未經高溫儲存測試之矽晶片接合於具鎳鍍膜軟板試片，剪力測試後 (a)軟板端破斷面，(b)矽晶片端殘留之金凸塊
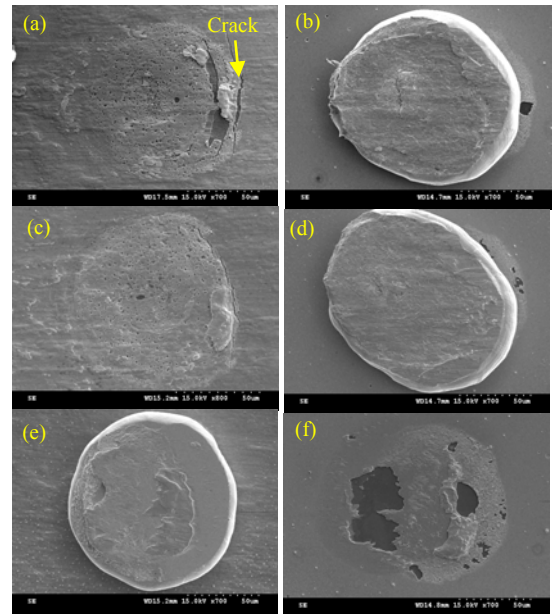
圖七 高溫儲存 1000 小時後，(a)軟板鍍膜拔離端破斷面，(b)矽晶片端殘留之金凸塊，(c)金凸塊於軟板表面剝離破斷面，(d)矽晶片端殘留之金凸塊，(e)金凸塊殘留於軟板，(f)金凸塊於矽晶片銲墊剝離
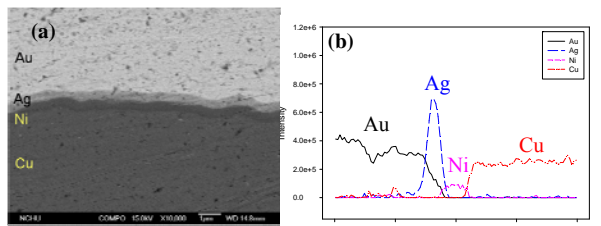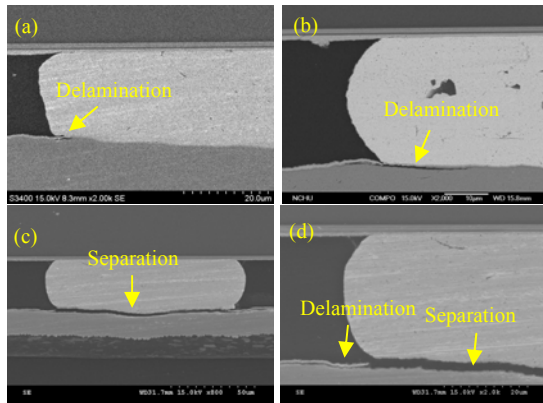

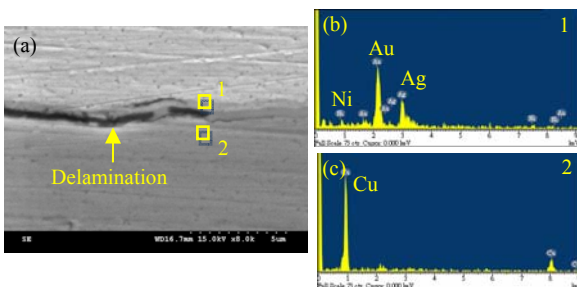圖八 高溫儲存 1000 小時候，金凸塊接合軟板銅電極之接合介面，(a)二次電子影相圖，(b)原子交互擴散圖
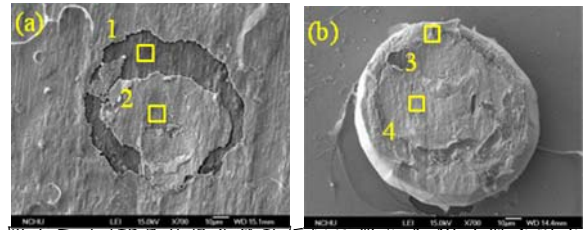
圖九 高溫蒸煮時數對剪力值之影響

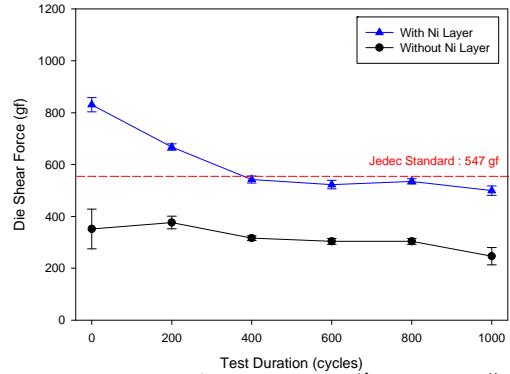圖十 矽晶片接合於軟性基板剪力測試後破斷面，經高溫蒸煮 (a)24 小時 (b)48 小時 (c) 96 小時 (d)336 小時

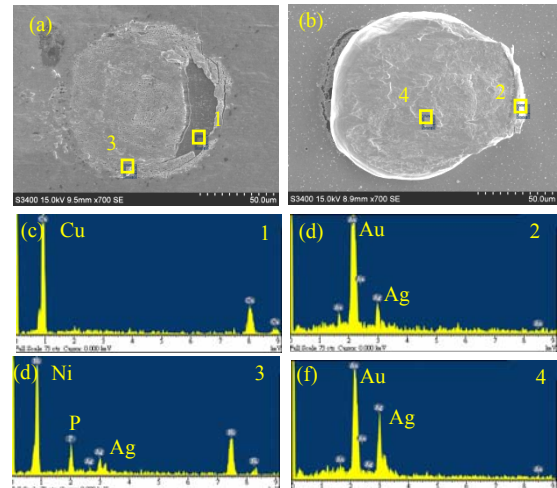圖十一 矽晶片接合於軟性基板之橫截面圖，經高溫蒸煮 (a)24 小時 (b)48 小時 (c)336 小時 (d)336 小時

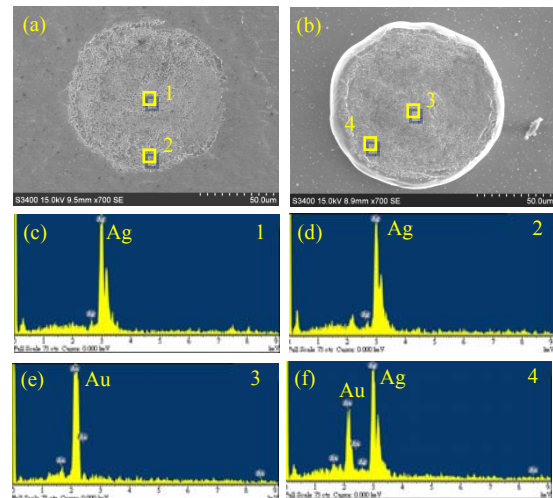圖十二 (a)矽晶片接合於軟板經高溫蒸煮 48 小時之橫截面， (b) point 分析圖譜，(c) point 2 分析圖圖譜

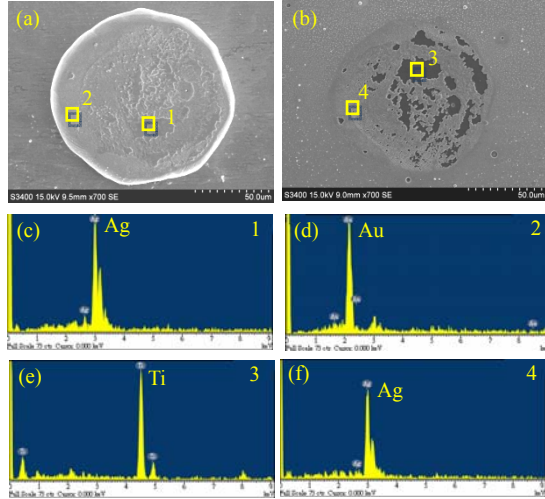圖十三 (a)矽晶片接合於軟板經高溫蒸煮 48 小時之剪力測試後軟板斷面圖， (b)殘留於晶片端之金凸塊

圖十四 溫度循環週期對剪力值之影響

圖十五 溫度循環 1000 週期後，銅電極鍍膜拔離之破斷面(a)軟性基板端破斷面，(b)晶片端破斷面，(c) point 1 之能量光譜，(d) point 2 之能量光譜，(e) point 3 之能量光譜，(c) point 4 之能量光譜。

圖十六 溫度循環 1000 次，金凸塊與軟性基板接合界面剝離之破斷(a)軟性基板端破斷面，(b)晶片端破斷面，(c) point 1 之能量光譜，(d) point 2 之能量光譜，(e) point 3 之能量光譜，(c) point 4 之能量光譜。

圖十七 溫度循環 1000 次，金凸塊由晶片銲墊剝離之破
斷面，(a)軟性基板端破斷面，(b)晶片端破斷面，
(c) point 1 之能量光譜，(d) point 2 之能量光譜，(e)
point 3 之能量光譜，(c) point 4 之能量光譜。
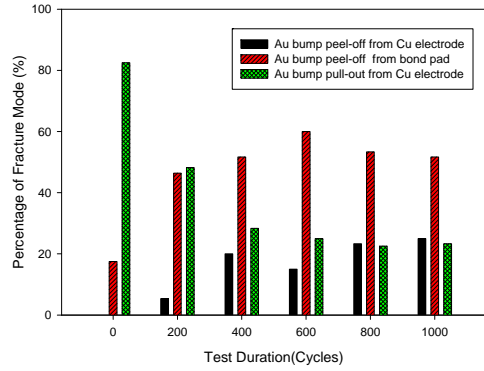
圖十八 溫度循環週期對剪力測試後斷裂模式之統計
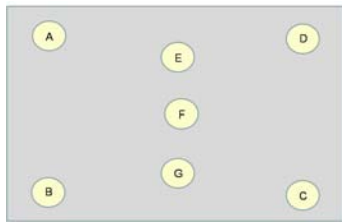
圖十九 晶片上金凸塊分佈示意圖
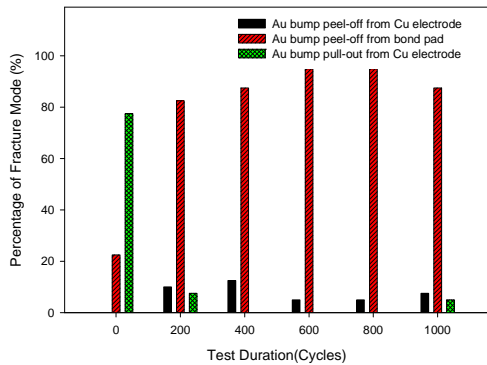
圖二十 晶片外側金凸塊經溫度循環週期與剪力測
試後斷裂模式之統計圖
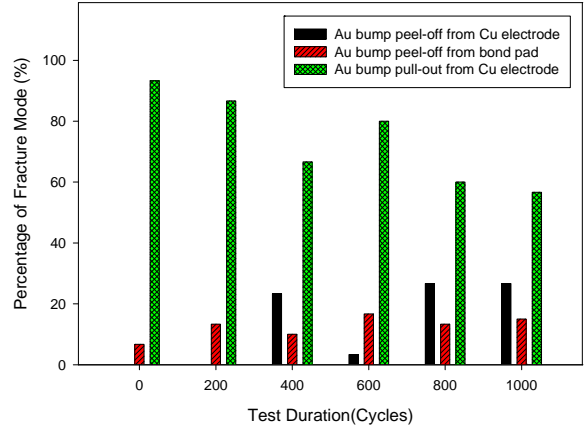
圖二十一 晶片中央金凸塊經溫度循環週期與剪力測試
後斷裂模式之統計圖

圖二十二 試片經不同週期之溫度循環測試後，矽晶片
接合於軟板之橫截面，(a)200 週期，(b)1000 週期

圖二十三 試片溫度循環 1000 週期後，矽晶片接合於軟
板橫截面，(a)晶片中央接點，(b)晶片外圍接點
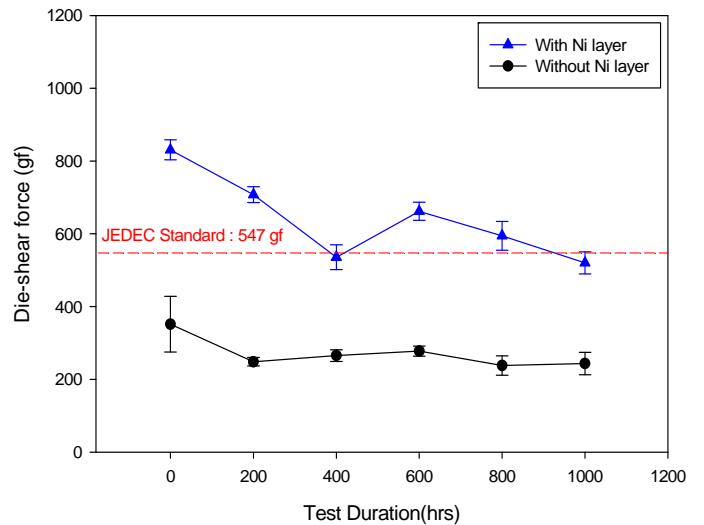
圖二十四 恆溫/恆濕測試時數對剪力值之影響
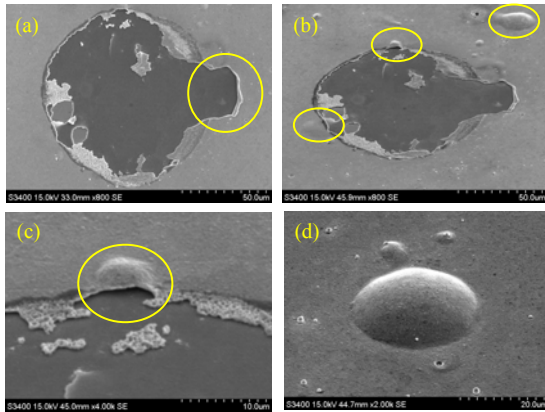
圖二十五 恆溫/恆濕測試 1000 小時後,(a)矽晶片銲墊破斷
　　　　面, (b)傾角 30 度觀察破斷面,(c)金凸塊接著區域周
　　　　圍之氣泡,(d)晶片銲墊鍍膜之氣泡
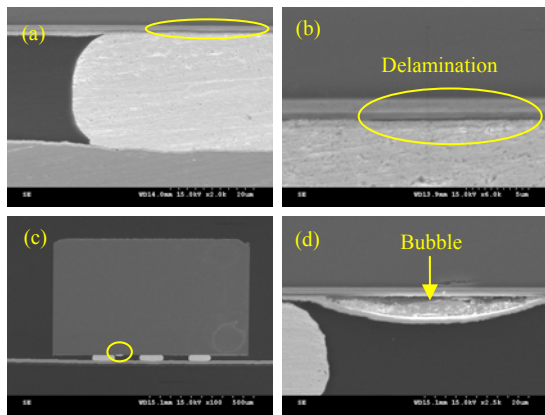
圖二十六 矽晶片接合於軟板橫截面,經恆溫/恆濕測試
　　　　(a)200 小時,(b)200 小時脫層缺陷局部放大,(c)400
　　　　小時,(d)400 小時氣泡局部放大

出席國際學術會議心得報告

<div align="right">100 年 9 月 10 日</div>

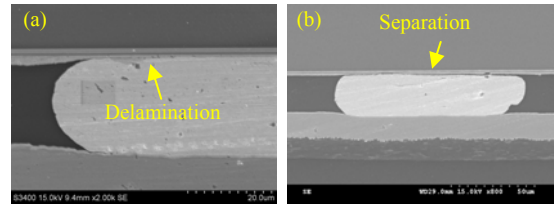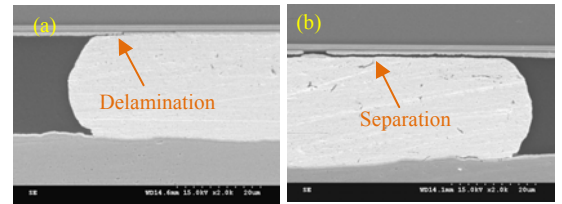| 報 告 人 姓 名	莊正利	系 所 單 位 ／ 職 稱	中山醫學大學職業安全衛生學系 副教授
會 議 期 間	Aug 8-11, 2011	會 議 地 點	Shanghai, China
主辦會議機構	China Semiconductor Industrial Association		
會 議 名 稱	(中文)2011 微電子構裝與高密度封裝國際會議 (英文)2011 International Conference on Electronic Packaging Technology & High Density Packaging		
發表論文題目	(中文) (英文) Enhancements of Bondability and Die-Shear force of Chips Thermosonically Bonded to Flex Substrates by Depositing a Nickel Layer		
所 屬 領 域	工程		

<div align="center">報　　告　　內　　容</div>

一、參加會議經過：

　　本次微電子構裝國際學術會議係由大陸半導體協會主辦，並由上海大學微電子研究所承辦，會議時間為 8 月 8 日至 11 日共 4 日，因部分封裝廠均於大陸上海郊區、蘇州等地設立封裝廠，而且規模遠大於台灣，故微電子構裝技術在大陸蓬勃發展，被視為新興科技工業，產、官、學界投入大量人力、物力與財力發展封裝技術，並透過投資優惠吸引台商於該地設立封裝廠，如此次研討會之主要贊助商日月光即是一例。為滿足求知若渴工程師、研究生，主辦單位在 8 月 7 日至 8 日舉辦微電子構裝技術之短期課程，內容涵蓋微電子構裝之發展趨勢、材料之應用、生產技術之提升與可靠度相關驗證等。今年會議主題與往年大致相同，可分為八大項：Advanced Packaging & System Integration、Packaging Materials & Process、 Packaging Design and Modeling、High Density & SMT、Advanced Manufacturing & Packaging Equipment、Quality & Reliability、Solid State Light Packaging and Integration、Emerging Technologies。因大陸具有廣大消費市場，故各大微電子廠商紛紛前往大陸設廠，因此，在會議中不乏來自台灣的贊助廠商或構裝業者。本次會議參加人數達 600-700 人，四處可見各廠商之技術、研發人員穿梭於議場，尋找對其發展有利之關鍵生產技術，可見微電子構裝產業在大陸蓬勃發展，也可預見不久將來，對岸微電子構裝技術必然突飛猛進，甚至超越台灣的發展。

二、與會心得：

　　主辦單位將議程第一天安排微電子構裝技術各領域專家進行專題演講，邀請學者亦和往年相似，包括知名國際期刊 Microelectronic Reliability 主編 Michael Pecht 教授、日本東京大學 Tadastomo Suga 教授與 Rao Tummala 教授等，其中 Michael Pecht 教授提到目前消費性電子種類繁多，功能差異性大，發展趨勢為輕、薄、短、小，對元件或是系統之可靠度更是形成嚴重挑戰，並且業界泛用之 JEDEC Standards 也有超過 40 年，部分規範未隨發展技術之提升而修改，顯然無法符合目前微電子設備之發展需求，他也會議中，期勉所有參與微電子構裝技術發展的專業人士，能投入更多心力於可靠度之研究；而在構裝接合技術方面，來自日本 Suga 教授過去曾提出「**自我活化接合(Self activated bonding ;SAB)**」技術，從傳統接合技術常用之熱壓接合(thermal compression bonding)、超音波接合(ultrasonic bonding)或熱音波接合(thermosonic bonding)轉換置凸塊(bump)與銲墊(bond pad)於常溫接合，但該技術需於高度真空下進行金凸塊與電極之接合，學術上雖取得豐碩的研究成果，但運用於實際生產作業中卻是困重重，所以今年 Suga 教授於演講中展示其實驗室目前正在研究主題，於大氣環境、室溫環境中接合矽晶片與基板(substrate)，於金屬凸塊(bump)與金屬電極(electrode)表面植入數層原子尺度之鐵離子，該鐵離子可使金凸塊與金屬電極有機會在大氣、室溫環境下接合，雖然 Suga 教授表示該技術仍未完全成熟，但在實驗室中已取得成功接合之樣品，但詳細接合機制仍未完全掌握，亦期待有興趣同好加入此一領域之研究。

　　此次會議發現比起前年(2009)於北京清華大學參加此一研討會，相較之下對岸之研究主題已由過去技術層次較低之銲線(wire bonding)封裝製程轉換成技術較高 3-D 堆疊技術，不僅是生產技術研究論文數量提高，甚至部分機理或理論之推導論文數量亦相對提升，相形之下，台灣在封裝相關技術上保有之領先程度已逐漸縮短，而且由各重點大學(清華、北大、哈爾賓、上海等)提供相關經費研究，教師、研究生或專業工程師熱烈參與封裝技術之相關研究，可預見封裝技術在對岸官方、學界與業界大力支持發展下，將超越台灣目前所保有之領先程度。

三、具體建議：

1. 整體而言，該研討會算是相當成功，不僅國外專業人士投稿數量或品質均相當不錯，且會議流程與周邊配合事項比起前年大幅進步。
2. 整個會議論文均提交登載於 IEEE 會議論文，若有國際知名學術期刊選擇品質較佳文章登載，應可提升參與發表論文品質。
3. 參加國際會議除可培養國際觀外，更可與各領域傑出研究者討論，可提升研究能量，建議國科會應儘量補助研究人員參與國際學術會議。

五、攜回資料名稱及內容：

1. ICEPT-HDP 2011 PROCEEDINGS(ISBN:978-1-4577-1768-0)
2. SEMICONDUCTOR MANUFACRURING (ISSN:1555-9270)
3. EQUIPMENT FOR ELECTRONIC PRODUCTS MANUFACTURING (ISSN:1004-4507)

六、附件：

　　登載於 IEEE 資料庫之會議論文(如後所示)。

七、活動照片(具代表性之活動照片)：

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報告人簽章：　　　莊正利

Enhancements of Bondability and Die-Shear force of Chips Thermosonically Bonded to Flex Substrates by Depositing a Nickel Layer

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Abstract

The purpose of this study was to investigate the influence of the nickel layer on the bondability and die-shear force of chips and flex substrates they were assembled using thermosonic flip-chip process. The copper electrodes over the flex substrate that were electroplated with a 0.5μm-thick nickel layer on the surface of copper film and the silver film was then deposited on the nickel layer to be as the bonding layer. This nickel layer was expected to improve the bondability and die-shear force of the assembly of chips that were thermosonically flip-chip bonded on the flex substrates. The thermosonicially flip-chip bonded experiments were conducted using an automatic thermosonic flip-chip bonder developed by ITRI. After chips bonded on the flex substrates, a subsequent die-shear test was performed to evaluate the bonding quality according to the JESD22-B116 standard.

Chips were successfully thermosonically flip-chip bonded on the copper electrodes that deposited with a 0.5μm-thick nickel layer using the adequate parameters. 100% bondability can be obtained and the die-shear force was higher than the minimum required values stated in the JEDEC standards for the assembly of chips they were thermosonically flip-bonded on copper electrodes with depositing a 0.5μm-thick nickel layer. A poor bondability and low die-shear force were existed when chips thermosonically flip-bonded on the copper electrodes that the nickel layer without depositing on them. According to observation on the surface morphology of the copper electrodes that were deposited with the nickel layer, a clear bonding trace can be observed, indicating the nickel layer was effective to improve propagation of the ultrasonic power to the bonding interface between the copper electrodes and the gold bumps. Enhancing the bonding quality of the assembly of chips and substrates during thermosonically flip-chip bonded process. Both bonability and the die-shear force are thus improved. In this study, the adequate bonding parameters of chips they were thermosonically flip-bonded to the flex substrates were an ultrasonic power of 20.66 W, a bonding force of 625 gf, a bonding time of 0.3 s and a bonding temperature of 200°C.

Deposition of the 0.5μm-thick nickel layer on the copper electrodes over flex substrates is effective to improve the bondability and die-shear forces of the assembly of chips they were thermosonically flip-bonded on the flex substrates.

Keywords: Thermosonic flip-chip bonding, Flex substrate, Nickel layer.

Introduction

The flex substrates have been widely used in consumed electronic products due to their flexibility and lighter than those of the rigid substrates. However, the thermal stability and mechanical properties of flex substrates are inferior to those of rigid substrates. Several challenges must be overcome before flex substrates can be used in the packaging of electronic products. For example, the thermosonic flip-bonded process is difficult to be applied to the assembly of chips and flex substrates. The temperature of the thermosonic bonding of gold balls onto rigid substrates is approximately 200°C [1]. Most flex substrates soften at such an elevated bonding temperature and dynamic sinking therefore occurs during thermosonic bonding [2]. Furthermore, the ultrasonic power could not propagate to bonding interface between the gold ball and the copper electrodes, and the bonding efficiency of the ultrasound is thus reduced. The gold ball cannot well bond on the copper electrode over the flex substrate [3].

In a flip-chip-on-flex (FCOF) assembly, the anisotropic conductive paste (ACP) and the non-conductive paste (NCP) were added to bind the chip and flex substrate [4, 5]. To obtain a sound bond with the sufficient bonding strength between the chips and the flex substrate, the curing time and curing temperature should be precisely controlled. These features in adhesive binding process would increase the manufacturing cost in the electronic packaging. Therefore, a direct bonding process for the assembly of chips and flex substrates is required. In general, there are three categories of bonding process have been used in direct assembly of silicon chips and rigid substrates, thermal compression bonding, ultrasonic bonding and thermosonic bonding, respectively. The major bonding energy of thermal compression bonding process was thermal energy and bonding load. Nave *et. al* [6] has point out that the bonding parameters of silicon device flip-bonding on the ceramic substrates using the thermal compression bonding process were 0.5 N in bonding load for each bump and 300°C in bonding temperature. At this elevated bonding temperature, the thermal stress would be formed at bonding interface and the electronic device could be damaged. The ultrasonic power is the major energy source of the ultrasonic bonding process. The bonding quality is highly depended on the ultrasonic power. Too small ultrasonic power is insufficient to produce good bonding quality between chips and substrates. A crating could be formed underneath the bond pads when an excessive ultrasonic power was applied to assemble the chips and substrates. Therefore, the ultrasonic power should be controlled in the moderate range in the ultrasonic bonding process. The thermosonic bonding process combines two energy sources, ultrasonic power and thermal energy. This bonding process is a matured process for the assembly of chips and rigid substrates. However, the thermosonic bonding process is difficult to be applied to the assembly of chips and flex substrates directly since the dynamic sinking occurred at

flex substrates during thermosonic bonding process. The ultrasonic power could not be transferred to the bonding interface to form a sound bond with sufficient bonding strength between the gold bumps and the copper electrodes. The bondability and die-shear force of the assembly of chips and flex substrates cannot meet the minimum requirements stated in the industrial codes. It is thus essential to improve the rigidity of flex substrates before the thermosonic bonding process was applied to the assembly of chips and flex substrates.

Deposition of a 0.5μm-thick nickel layer on the surface of copper electrodes is an effective way to improve the bondability and bonding strength of a gold ball bonded on the copper electrodes over the flex substrates using the thermosonic wire bonding process [3]. This nickel layer was shown which can improve the rigidity of copper electrodes over the flex substrate and the ultrasonic power can be successfully transferred to bonding interface between the gold ball and the copper electrode. The bondability and bonding strength are thus improved. However, this method was limited to single gold ball that were thermosonically bonding to copper electrode over the flex substrate. No public literature was found to provide an effective scheme to be applied to assemble the chips and flex substrates directly using the thermosonic flip-chip bonding process. This work thus attempts to assemble the chips and flex substrates directly using the thermosonic flip-chip bonding process. A nickel layer of 0.5μm-thick was deposited on the surface of copper electrodes over the flex substrates, and this nickel layer is expected to improve the rigidity of copper electrodes over flex substrates, and then to enhance the bondability and die-shear force.

Experimental method

A commercial flex substrate of polyimide (PI) was used in this investigation and the copper layer was deposited on the surface of flex substrates as a copper electrode. To examine the effect of the nickel layer on the die-shear force and bondability of the assembly of chips and flex substrates using thermosonic flip-chip bonding process, the specimen was divided to two categories, one is copper electrodes without the nickel layer deposited, and the other is copper electrodes depositing with the 0.5μm-thick nickel layer. Finally, the 0.5μm-thick silver layer was deposited on the surface of each copper electrode as a bonding layer to improve the bondability and bonding strength [7]. The stacking sequence of the former copper electrode was Ag/Cu/PI from top to bottom and the latter copper electrodes comprised a nickel layer that was deposited between the copper layer and the silver layer. The stacking sequence of the latter copper electrode was Ag/Ni/Cu/PI. These deposited layers were electroplated on the surface of copper film. A automatic stud bump bonder was employed for gold stud bumping onto copper pads and the bumping parameters have been described in authors' previous work [8]. After gold stud bumping, the bumped wafer was diced into chips with 1.19 mm x 0.97 mm; each has eight gold stud bumps.

The bonding experiments of chips studded with gold stud bumps they were thermosonically flip-bonded onto copper electrodes over the flex substrates were carried out on an automatic thermosonic flip-chip bonder developed by the Industrial Technology Research Institute (ITRI). The major parameters, bonding load, ultrasonic power and bonding time for used in the assembly of chips and substrates are investigated in this study. After chips bonded on the flex substrates, the die-shear test was carrier out using a Royce 552 tester to evaluate the die-shear force in a manner consistent with EIA/JEDEC JESD22-B116 standard [9]. There are at least 15 specimens that were tested to obtain an average die-shear force for each bonding condition.

Scanning electron microscope (SEM) was used to measure the diameter of the gold bumps they were bonded on the copper electrodes and to investigate the bonding interface between the bumps and the copper electrodes. After die-shear test, the SEM and an energy dispersive spectrometer (EDS) were adopted to examine the fracture morphology after die-shear test, and to elucidate the fracture mechanism of the assembly of chips and flex substrates using thermosonic bonding process.

Results and discussion

Effects of ultrasonic on the bondability and die-shear force

The ultrasonic power plays an important role to assemble the chips and flex substrates using the thermosonic bonding process. To verify the effect of ultrasonic power on die-shear force of the assembly of chips and flex substrates, the ultrasonic powers are varied from 0 W to 36.2 W and others bonding parameters are fixed (bonding load in 625 gf, bonding time in 0.5 s and bonding temperature at 200°C). The bondability in this study was defined that the number of chips bonded on the flex substrates divided by the total number of bonding actions. Figure 1 presents the bondabilty of chips and flex substrates they were assembled at various ultrasonic powers. The bondabilty is 0 for chips they were bonded to copper electrodes with the nickel layer and to copper electrodes without the nickel layer when the applied ultrasonic power was 0 W. No chip can be successfully bonded on the copper electrodes over the flex substrates at 0 W of ultrasonic power. This experimental result indicates that the chips and flex substrates cannot be successfully assembled using the thermal compression bonding process and the ultrasonic power plays an important role for the assembly of chip
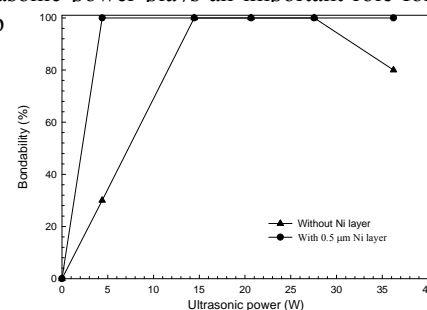
Figure 1 Relationships between the ultrasonic power and the bondability of the assembly of chips they were bonded to copper electrodes with the nickel layer and to copper electrodes without the nickel layer. Bonding parameters were 625 gf in bonding load, 0.5 s in bonding time, 200°C at bonding temperature, and the ultrasonic powers were varied from 0 W to 36.22 W.

As increase the ultrasonic power to 4.4 W, the bondability of chips they were thermosonically bonded to copper electrodes without nickel layer only approximately 30%. Most of chips cannot be bonded on the copper electrodes, and the bonding marks with limited scrapes left on the surface of copper electrodes over the flex substrates, as shown in Fig. 2(a). It well known the scraping traces on the surface of copper electrodes over the flex substrates was made by the vibration of ultrasonic power during thermosonic bonding process. Therefore, the bonding marks with the limited scraping traces imply that the ultrasonic power at the bonding interface between the gold bumps and the copper electrodes was not sufficient to form the sound bonds. The low ultrasonic power of 4.4 W results in a poor bondability of chips they were thermosonically bonding to copper electrodes without depositing the nickel layer. In contrast to a poor bondabilty of chips and copper electrodes without depositing the nickel layer they were assembled using a low ultrasonic power of 4.4 W, 100% bondability can be achieved using a low ultrasonic power of 4.4 W for the assembly of the chips and copper electrodes depositing with a 0.5μm-thick nickel layer over the flex substrates. All tested chips were successfully bonded on the copper electrodes depositing with the nickel layer over the flex substrates as shown in Fig. 2(b). The nickel layer deposited on the copper electrodes was effective in improving bondability of chips they were thermosonically bonding to copper electrodes over the flex substrates at low ultrasonic power. In authors' previous study has been verified that the rigidity of a copper electrode over the flex substrate can be strengthen by depositing a nickel layer on its surface and this nickel layer improved the bondability of a gold ball it was thermosoniclly bonding to the copper electrode over the flex substrate [3]. The nickel layer could enhance the propagation of the ultrasonic power from chips to the bonding interface, and the bondability was thus improved.
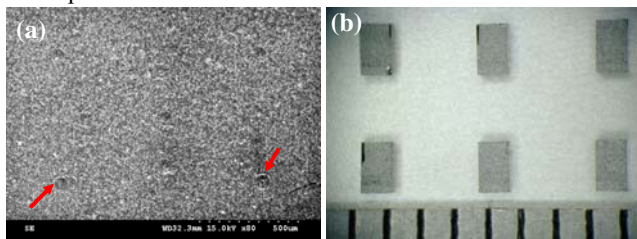

Figure 2 The micrographs show the surface morphology of chips they were thermosonically bonding to (a) copper electrodes without depositing the nickel layer using ultrasonic power of 4.4 W, (b) copper electrodes with 0.5μm-thick nickel layer using ultrasonic power of 4.4W. Others parameters were 625 gf in bonding load, 200°C in bonding temperature and 0.5s in bonding time.

For the ultrasonic power was varied from 14.46 W to 27.56 W, the bondability of the assembly of chips and flex substrates maintained at 100%, implying all the chips were successfully bonded on the both test specimen, copper electrodes without depositing the nickel layer and copper electrodes depositing with the nickel layer. Increasing the ultrasonic power provides the sufficient bonding energy at

bonding interface, and the perfect bondability can be obtained. However, the bondability of chips they were thermosonically bonding to copper electrodes without the nickel layer reduced to 80% when the applied ultrasonic power increased to 36.22 W. An excessive ultrasonic power applied to copper electrodes without depositing the nickel layer could not be formed a firm contact between the gold bumps and the copper electrodes, and then the ultrasonic power could hard to propagate to the bonding interface during the thermosonic flip-chip bonding process. The bondability is thus degraded. One hundred percent bondability was shown in Fig. 1 for chips they were thermosonically bonding to copper electrodes with depositing the nickel layer at high ultrasonic power of 36.22 W. Depositing a nickel layer on the copper electrode improved the elastic modulus. The elastic modulus increased with the thickness of the nickel layer from 68.7 GPa with no such layer to 108 GPa when a 0.5μm-thick nickel layer was deposited on the copper electrode [3]. Therefore, the 0.5μm-thick nickel layer deposited on the copper electrodes over the flex substrates could enhance the rigid contact between the gold bumps and copper electrodes for a high ultrasonic power of 36.22 W applied to bonding process, and the perfect bondability can be maintained.

Deposition of the 0.5μm-thick nickel layer on the copper electrodes over the flex substrates is an effective way to improve the bondability of the assembly of chips and flex substrates. Based on the experimental results, two advantages can be obtained as follows; the first is that the nickel layer enhances the propagation of the ultrasonic power to the bonding interface for a low ultrasonic power of 4.4 W was applied to bonding process. The other is that the nickel layer could improve the rigidity of copper electrodes over the flex substrates and could provide a firm contact between the gold bump and the copper electrode for a high ultrasonic power of 36.22 W was applied to the thermosonic bonding process.

To examine the influence of the ultrasonic power on the die-shear force, each chip with eight gold studded bumps was thermosonically flipped-bonding to flex substrates at different ultrasonic powers. The thermosonic bonding parameters were 625 gf in bonding force, 0.5 s in bonding time, 200°C in bonding temperature and the ultrasonic power varied from 0 W to 36.22 W. Figure 3 presents that the die-shear force of chips they were thermosonically bonding to copper electrodes with the nickel layer and to copper electrodes without depositing the nickel layer increases with the ultrasonic power form 0 to 20.66 W, and then decreases with the ultrasonic power is further increased from 27.56 to 36.22 W. The bondability of the assembly of chips and flex substrates is zero when the applied ultrasonic power was 0 W, no die-shear force can be thus obtained. It is well known that the minimum required die-shear force stated at JEDEC standards is highly depended on the contact area at bonding interface between the bumps and the copper electrodes. In this study, the average contact diameter of the bonded bumps at different ultrasonic power was measured using SEM as shown in Fig. 4. At low ultrasonic power of 4.4 W, the average contact diameters of bonded bumps after chips they were thermosonically bonded on copper electrodes with the nickel layer and on copper electrodes without the nickel layer were approximately 75μm

and 72μm, respectively. An minimum ball-shear value stated in JEDEC standards is 30.8 gf for each ball bond when the diameter is 76.2μm (3.0 mil) and the 26.5 gf for each ball bond when the diameter is 71μm (2.8 mil). For each chip has eight gold studded bumps, a reasonable average die-shear force of each chip they was bonded to the copper electrodes with the nickel layer should be at least 246.4 gf and to the copper electrodes without the nickel layer should be higher than 212 gf for a low ultrasonic power of 4.4 W was applied to the bonding process. The average die-shear force of chips they were bonded on copper electrodes with the nickel layer is approximately 340 gf when an ultrasonic power of 4.4W was applied to the bonding process, as shown in Fig. 3. This average die-shear value was higher than that stated in the JEDEC standards. However, the average die-shear force of chips they were bonded on the copper electrodes without depositing the nickel layer is far below the minimum required value stated in JEDEC standards when the ultrasonic power of 4.4 W was applied to the bonding process. Deposition of the nickel layer on the copper electrodes was an effective way to improve the die-shear force of the assembly of chips and flex substrates at a low ultrasonic power of 4.4W.
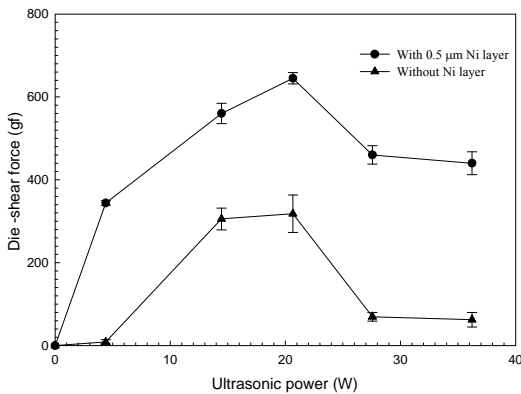

Figure 3 Influence of the ultrasonic powers on the die-shear force of the assembly of chips they were bonded to copper electrodes with the nickel layer and to the copper electrodes without the nickel layer. Bonding parameters were 625 gf in bonding load, 200°C in bonding temperature and 0.5s in bonding time.
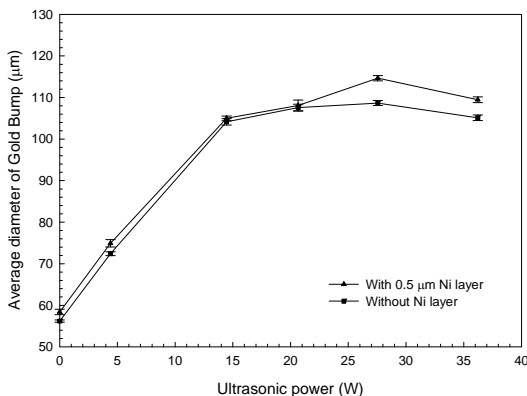

Figure 4 Relationships between ultrasonic powers on the average diameter of gold bumps they were thermosonically to copper electrodes with the nickel layer and to copper electrodes without the nickel layer. Bonding parameters were 625 gf in bonding force, 0-36.22 W in ultrasonic power, 200°C at bonding temperature and 0.5s in bonding time.

Increasing the ultrasonic power to 14.4 W, both the average diameters of bonded bumps rapidly rose to approximately 104μm after chips they were thermosonically boned on the copper electrodes with and without the nickel layer, as shown in Fig. 4. The minimum average required value stated in JEDEC standard is 493 gf when the average diameter of bonded bumps was 104μm. As the die-shear forces given in Fig. 3, the die-shear forces of chips they were thermosonically bonded on copper electrodes with and without the nickel layer were 560 gf and 300 gf, respectively. This die-shear force of the assembly of chips and copper electrodes with the nickel layer is higher than those stated in JEDEC standards. Similar analytical method was conducted to comparison of the experimental results shown in Figs. 3 and 4, the average diameter of the ball bonds and the die-shear force are both increased at the ultrasonic power of 20.66 W. No significantly difference in average diameters of gold bonds was observed in Fig. 4 between chips they were thermosonically bonded on copper electrodes with nickel layer and on the copper electrodes without the nickel layer, both of them are approximately 108μm. The highest die-shear forces appeared at the ultrasonic power of 20.66 W among various ultrasonic powers for chips they were thermosonically bonded on copper electrodes with and without the nickel layer. The die-shear force of the assembly of chips and copper electrodes with the nickel layer is 660 gf, which is higher than those of stated in JEDEC standards and the die-shear force of the assembly of chips and copper electrodes without the nickel layer, as shown in Fig. 3. As improve the ultrasonic power from 27.56 W to 36.22 W, both of the die-shear forces shown in Fig. 3 were degraded for chips they were thermosonically bonded to copper electrodes with the nickel layer and to copper electrodes without depositing the nickel layer. This experimental result reveals that the excessive bonding power could degrade the die-shear forces and the appropriate bonding parameters are essential to obtain the sufficient die-shear force.

Depositing of the 0.5μm-thick nickel layer on the copper electrodes over the flex substrate was effective to improve the die-shear forces of chips they were thermosonically bonded on them. A sufficient die-shear force can be achieved at the ultrasonic power of 20.66 W in this study. The insufficient and the excessive bonding power were deleterious to die-shear forces.

Effects of bonding load on the die-shear force

To investigate the degradation of die-shear forces at the ultrasonic power of 36.22 W, the bonding interface between the gold bumps and copper electrodes was shown in Figs. 5 and 6. Figure 5(a) displays the cross-section of a chip bonded on the copper electrode with depositing the nickel layer at ultrasonic power of 36.2 W. A delamination exists at bonding interface between the gold bump and the copper electrode as shown in Fig. 5(b). The serious delamination can be found at the interface between the bond pad of the chip and the gold bump and the interface between the gold bump and the copper electrode after chips they were thermosonically bonded to copper electrodes without depositing the nickel layer at the

ultrasonic power of 36.2 W as shown in Figs. 6(a) and (b). This experimental result indicates that bonding power was excessive and the bonding load seemed insufficient to keep a firm contact between the gold bumps and the copper electrodes.
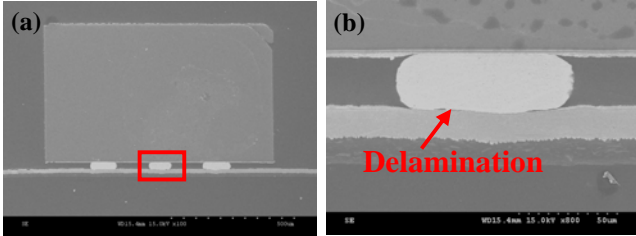

Figure 5 SEM micrographs of (a) the cross-section of gold bumps thermosonic bonded on the copper electrodes with the nickel layer and (b) larger magnification at bonding interface revealing a delamination formed between the gold bump and the copper electrode. Bonding parameters were 625 gf in bonding load, 36.22 W in ultrasonic power, 200°C at bonding temperature and 0.5 s in bonding time.
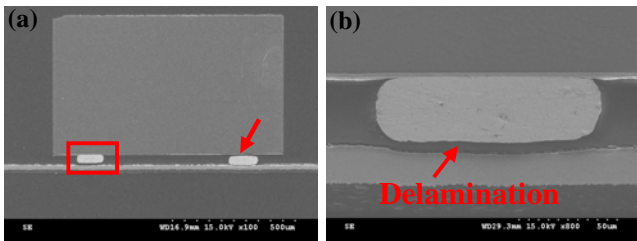

Figure 6 SEM micrographs of (a) the cross-section of gold bumps thermosonic bonded on the copper electrodes without depositing the nickel layer and (b) larger magnification at bonding interface revealing a serious delamination formed between the gold bump and the copper electrode. Bonding parameters were 625 gf in bonding load, 36.22 W in ultrasonic power, 200°C at bonding temperature and 0.5 s in bonding time.

As increase the bonding load to 925 gf, the sound bonding interface can be achieved at ultrasonic power of 36.22 W after chips they were thermosonically bonded on copper electrodes with the nickel layer and on the copper electrodes without the nickel layer as shown in Figs. 7 and 8, respectively. These observations can be used to interpret why the degradation of die-shear force at the range of the ultrasonic powers from 27.56W to 36.22 W, as shown in Fig. 3. The bonding energy of the ultrasonic power at the range of 27.56W to 36.22 W was excessive and the bonding force at 625 gf was insufficient to maintain a firm contact between the gold bumps and the copper electrodes. The ultrasonic power could not be transferred to the bonding interface to produce a sound bond with the sufficient die-shear force. This experimental result indicates that increasing bonding load appropriately is essential when a large ultrasonic power was applied to thermosonic bonding process.
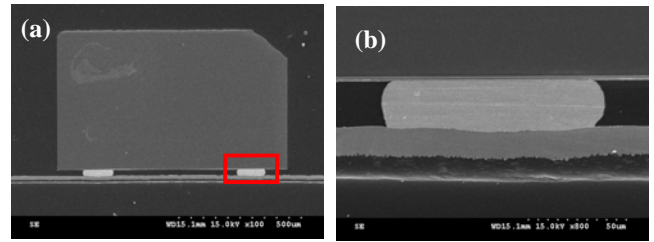

Figure 7 SEM micrographs of (a) the cross-section of gold bumps thermosonic bonded on the copper electrodes with the nickel layer and (b) larger magnification at bonding interface revealing a sound bond formed between the gold bump and the copper electrode. Bonding parameters were 930 gf in bonding load, 36.22 W in ultrasonic power, 200°C at bonding temperature and 0.5 s in bonding time.
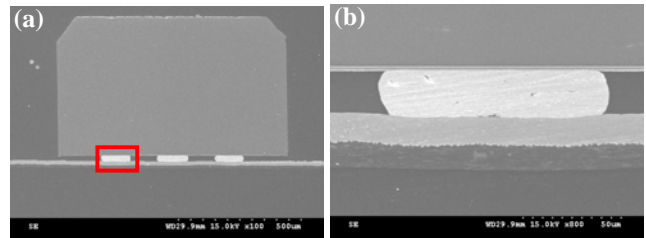

Figure 8 SEM micrographs of (a) the cross-section of gold bumps thermosonic bonded on the copper electrodes without depositing the nickel layer and (b) larger magnification at bonding interface revealing a sound bond formed between the gold bump and the copper electrode. Bonding parameters were 930 gf in bonding load, 36.22 W in ultrasonic power, 200°C at bonding temperature and 0.5 s in bonding time.

Effects of bonding time on the die-shear force

The SEM was used to examine the bonding interface between the gold bumps and the copper electrodes for the assembly of chips and flex substrates at ultrasonic power of 20.66 W, as shown in Fig. 9(a). A large magnification of the SEM micrograph shown in Fig. 9(b) displays that a slight delamination can be found at the interface between the bond pad of chips and gold bumps after chips they were thermosonically bonded on copper electrodes with the nickel layer. This delamination could decrease the service life of chips. A short bonding time of 0.3 s was thus choice to be applied to the thermosonic bonding process. A die-shear force of the assembly of chips and flex substrates was approximately 600 gf and the average contacted diameter of gold bumps was 102 um at bonding time of 0.3 s. The minimum requirement stated in JEDEC standard is approximately 466 gf when the contacted diameter was 102 um. This die-shear force is higher than those stated in the JEDEC standard. Neither the delamination nor defects was found at bonding interface of the assembly of chips and flex substrates at bonding time of 0.3 s shown in Figs. 10(a) and (b). This observation indicates that a sound bond without defects can be achieved by reducing the bonding time. This phenomenon can be explained by the interfacial energy

saturation [10]. Extending bonding time results a delamination forming at bonding interface, because an excessive bonding energy was provided. For 0.3 s in bonding time, a sound-bonding interface with no defects was observed and the die-shear force was higher than that stated in JEDEC standard. Although the die-shear force at bonding time of 0.5 s was higher than that at bonding time of 0.3 s, but reducing bonding time to 0.3 s not only to obtained a sound of bonding interface, and it can reduce the manufacturing time.
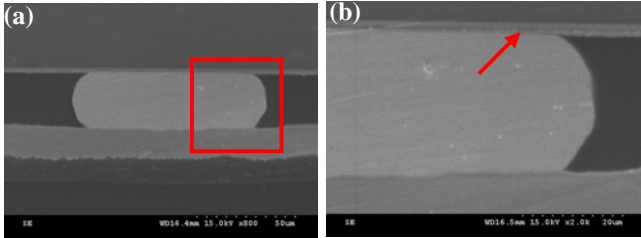

Figure 9 SEM micrographs of (a) the cross-section of the gold bump thermosonic bonded on the copper electrodes with the nickel layer and (b) larger magnification at bonding interface revealing a slight delamination formed between the gold bump and the copper electrode. Bonding parameters were 625 gf in bonding load, 20.66 W in ultrasonic power, 200°C at bonding temperature and 0.5 s in bonding time.
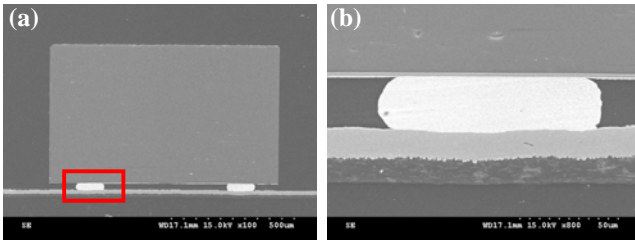

Figure 10 SEM micrographs of (a) the cross-section of gold bumps thermosonic bonded on the copper electrodes with the nickel layer and (b) larger magnification at bonding interface revealing a sound bond formed between the gold bump and the copper electrode. Bonding parameters were 625 gf in bonding load, 20.66 W in ultrasonic power, 200°C at bonding temperature and 0.3 s in bonding time.

Analysis of fracture morphology after the die-shear test

For chips they were thermosonically bonded on copper electrodes with depositing the nickel layer using a bonding time of 0.3 s, an ultrasonic power of 20.66 W, a bonding temperature of 200°C and a bonding load of 625 gf, Fig. 11 shows fracture morphology and an energy dispersive spectrum (EDS) on the copper electrode after the die-shear test. A residue on the surface of the copper electrode after die-shear test can be found as shown in Fig. 11(a). To examine the composition of the residue on the surface of the copper electrode, an EDS was used to determine the composition of the residue. The composition of the residue is mainly gold and a small amount of silver as given in Fig. 11(b). This analytical result implies that the fracture mode was the gold bumps fractured. The bonding strength of the assembly of chips and flex substrates are even higher than that of gold bumps. Figure 12 reveals the fracture morphology of chips they were thermosonically bonded on copper electrodes without

depositing the nickel layer using a bonding time of 0.3 s, an ultrasonic power of 20.66 W, a bonding temperature of 200°C and a bonding load of 625 gf. A round indention can be found on the surface of the copper electrode as given in Fig. 12(a). To verify the composition of this bonding indention on the surface of the copper electrode using an EDS, the main composition is silver as shown in Fig. 12(b). The fracture mode of the assembly of chips they were thermosonically bonded on the copper electrodes without depositing the nickel layer is a peel-off at bonding interface between the gold bumps and the surface of copper electrodes. The gold bump peeled-off from the surface of the copper electrode during the die-shear test, indicating the die-shear force is low. This experimental result proves again that high die-shear force was obtained for chips they were thermosonically bonded on copper electrodes with the nickel layer.
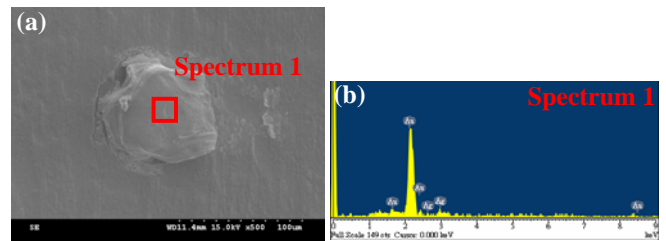

Figure 11 The SEM micrograph of (a) the fracture morphology of copper electrodes with a 0.5μm-nickel layer after die-shear test, (b) the EDS analysis on the residue left on the surface of the copper electrode. Bonding parameters were 625 gf in bonding load, 20.66 W in ultrasonic power, 200°C at bonding temperature and 0.3 s in bonding time.

Figure 12 The SEM micrograph of (a) the fracture morphology of copper electrodes without depositing a 0.5μm-nickel layer after die-shear test, (b) the analysis of the EDS on the round indention left on the surface of the copper electrode. Bonding parameters were 625 gf in bonding load, 20.66 W in ultrasonic power, 200°C at bonding temperature and 0.3 s in bonding time.
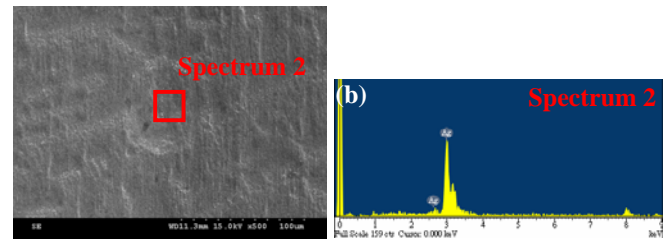
Observation of the bonding interface between the gold bumps and the copper electrodes

To observe the bonding morphology on the surface of copper electrodes, the assembly of chips and flex substrates was put in water bath, and then a large ultrasonic power was applied to separate the chips from the flex substrates. The SEM was used to verify the bonding morphology on the surface of copper electrodes after chips separating from flex substrates. For chips they were thermosonically bonded to copper electrodes with the nickel layer at various ultrasonic powers, the surface morphology of copper electrodes was shown in Fig. 13. A clear round indention with a diameter of 72 um approximately shown in Fig. 13(a) was observed for chips they were thermosonically bonded to copper electrodes

at ultrasonic power of 4.4 W. As increasing ultrasonic power to 20.66 W or 27.56 W, the deposited layers on the copper electrodes were pulled out to form caves as shown in Figs. 13(b) and (c), indicating the bonding strength between the gold bump and the copper electrode is higher than the adhesive strength between deposited layers of the copper electrode. This experimental result reveals again that high ultrasonic powers resulted in high die-shear forces of the assembly of chips they were thermosonically bonded to copper electrodes with the nickel layer, as mention in Fig. 3.
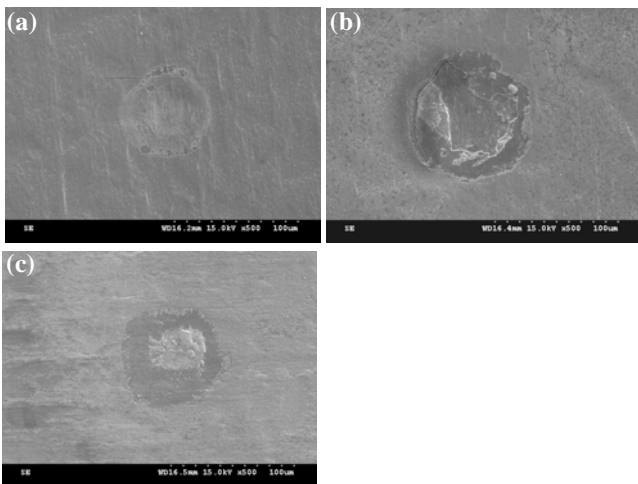

Figure 13 SEM micrographs of fracture morphologies on the copper electrodes after gold bumps separating from the surface of the copper electrodes. The assembly of chips they were thermosonically bonded on the copper electrodes with the nickel layer at various ultrasonic powers, (a) 4.4 W, (b) 20.66 W and (c) 27.56 W. Others parameters were 625 gf in bonding load, 200°C at bonding temperature and 0.3 s in bonding time.

In contrast to a round indention left on the surface morphology of copper electrodes for chips they were thermosonically bonded on the copper electrodes with depositing the nickel layer, neither scratches nor clear round indention was observed on the surface morphology of copper electrodes for chips they were thermosonically bonded on copper electrodes without depositing the nickel layer at various ultrasonic powers, as shown in Figs. 14(a), (b) and (c). It well known that high ultrasonic power results more scratches forming at bonding interface. Thus, more ultrasonic power was propagated to bonding interface for chips they were thermosonically bonded to copper electrodes with depositing the nickel layer. Deposition of the 0.5μm-thick nickel layer on the copper electrodes over the flex substrates are effective in improving the transmission of ultrasonic power to bonding interface, and the die-shear force of assembly of chips and flex substrates was enhanced.
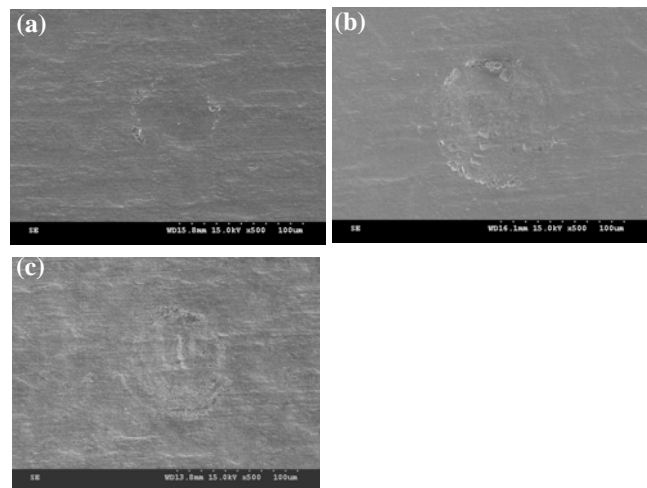

Figure 14 SEM micrographs of fracture morphologies on the copper electrodes after gold bumps separating from the surface of the copper electrodes. The assembly of chips they were thermosonically bonded on the copper electrodes without depositing the nickel layer at various ultrasonic powers, (a) 4.4 W, (b) 20.66 W and (c) 27.56 W. Others parameters were 625 gf in bonding load, 200°C at bonding temperature and 0.3 s in bonding time.

Conclusions

Deposition of the 0.5 μm-thick nickel layer on the copper electrodes over the flex substrates, the chips were successfully thermosonically bonded on the copper electrodes over the flex substrates. With the suitable bonding parameters, a perfect bondability and a high die-shear force of the assembly of chips and flex substrates can be achieved. This nickel layer was effective to enhance rigidity of copper electrodes, increasing the bonding efficiency of ultrasonic power at bonding interface between the gold bumps and copper electrodes during the thermosonically flip-chip bonded process. The bonding quality of the assembly of chips and flex substrates are thus improved. In this study, the adequate bonding parameters of the assembly of chips they were thermosonically bonded to the flex substrates were an ultrasonic power of 20.66 W, a bonding force of 625 gf, a bonding time of 0.3 s and a bonding temperature of 200°C.

As a large ultrasonic power was applied to the thermosonic bonding process, increasing bonding load is essential to make a firm contact between the gold bump and the copper electrode, and the ultrasonic power can be transferred successfully to the bonding interface between the gold bumps and the copper electrodess. The die-shear force is thus enhanced. Extending bonding time results a delamination forming at bonding interface, because an excessive bonding energy was provided. To obtain a sound bond with the sufficient bonding strength, the thermosonic bonding parameters should be controlled in a suitable range. According to the observation of the surface morphology of copper electrodes after chips they were separating from the copper electrodes, a round indention mark with the cavity was observed on the copper electrodes deposited with the nickel

layer, indicating the nickel layer is effective in propagating ultrasonic power to bonding interface between the gold bumps and the copper electrodes.

Deposition of the 0.5μm-thick nickel layer on the copper electrodes over flex substrates is effective to improve the bondability and the die-shear force of the assembly of chips they were directly thermosonically bonded on the flex substrates. This scheme has great potential to be applied to asemble the chips and flex substrates of electronic packaging.

Acknowledgments

References

1. C. L. Chuang, J. N. Aoh, Journal of Electronic Materials, 2006, Vol.33, No.4, p. 29.
2. G. G. Harman, "Wire Bonding in Microelectronics", McGraw-Hill,1997, p.267.
3. C. L. Chuang, H. F. Fan, Microelectronic Engineering, In press, 2011.
4. P. Palm, J. Maattanen, A. Tuominen and E. Ristolainen, Microelectronics Reliability, 2001,Vol. 40, p 633.
5. C. L. Chuang, Q.A. Liao, H. T. Li, S. J. Liao, G. S. Huang, Microelectronic Engineering, 2010, Vol. 87, p. 624.
6. J. Nave, Proceeding of ITAP, Sunnyvale, C.A. 1996, p.90.
7. C. L. Chuang, J. N. Aoh, Q. A. Liao, C. C. Hsu, S. J. Liao, G. S. Huang, Journal of Electronic Materials, 2008, Vol.37, No.11, p.1742
8. C. L. Chuang, Microelectronic Engineering, 2007, Vol. 84, p. 559.
9. JEDEC (EIA) Solid State Technology Product Engineering Council (Arlington, 1998).
10. Y. R. Jeng and J. N. Lin, Transactions of the ASME, Journal of Tribology, 2003,Vol.125, p. 578.

國科會補助計畫衍生研發成果推廣資料表

國科會補助計畫	計畫名稱: 矽晶片以熱音波能量直接覆晶接合於軟性基板銅電極之製程開發與機理研究(III)
	計畫主持人: 莊正利
	計畫編號: 99-2221-E-040-004-　　　　學門領域: 加工與製造

<table>
<tr><td colspan="2">無研發成果推廣資料</td></tr>
</table>

99 年度專題研究計畫研究成果彙整表

計畫主持人：莊正利　　計畫編號：99-2221-E-040-004-

計畫名稱：矽晶片以熱音波能量直接覆晶接合於軟性基板銅電極之製程開發與機理研究(III)

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	1	1	100%		
		研討會論文	2	1	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	1	1	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	2	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	1	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

計畫主持人：莊正利　　計畫編號：99-2221-E-040-004-

計畫名稱：矽晶片以熱音波能量直接覆晶接合於軟性基板銅電極之製程開發與機理研究(III)

	其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等,請以文字敘述填列。)	無		

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與(閱聽)人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

---

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

   ■達成目標

   □未達成目標（請說明，以 100 字為限）

       □實驗失敗

       □因故實驗中斷

       □其他原因

     說明：

---

2. 研究成果在學術期刊發表或申請專利等情形：

   論文：□已發表 ■未發表之文稿 □撰寫中 □無

   專利：□已獲得 □申請中 ■無

   技轉：□已技轉 □洽談中 ■無

   其他：（以 100 字為限）

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3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

   1.證明矽晶片與軟板接合可行性，除以鎳鍍層提高矽晶片與軟板之接合強度外，完成熱音波覆晶製程應用於矽晶片與軟板接合後之各項可靠度測試。

   2.矽晶片與軟板接合後之高溫儲存可靠度可通過相關規範之規定，但接合強度隨測試時間增長而逐漸降低，其原因為金凸塊與矽晶片銲墊間因熱膨脹係數之差異所引起之殘留熱應力所致；而高壓蒸煮試驗後之破壞機制為水氣侵入軟板銅電極之鍍膜，造成鍍膜間之剝離缺陷，引致接合強度之衰退；熱循環測試之者要破壞機理為高低溫循環引致金凸塊與矽晶片銲墊之熱膨脹係數差異，產生脫層之缺陷；恆溫/恆測試之主要破壞機理為濕氣侵入矽晶片銲墊表面形成氣泡，若該氣泡出現於金凸塊與銲墊接合區，接合強度出現大幅下降。

   3.由各項可靠度試驗建立之破壞機制，提供業界防範方法，有效提升晶片與軟板接合技術之可靠度。

   4.此一研究共建立四項測試之破壞機理，目前已完成論文撰寫，一篇已投稿 Microelectronic Engineering 期刊，另一篇預計近日內投至 Journal of electromic materials 期刊。