行政院國家科學委員會專題研究計畫 期末報告

以表面活化接合技術開發矽晶片與基板之室溫覆晶接合製程與其接合機理之研究

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計畫主持人：莊正利

計畫參與人員：碩士班研究生-兼任助理人員：楊博智

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公 開 資 訊 ：本計畫涉及專利或其他智慧財產權，1 年後可公開查詢

中 華 民 國 101 年 11 月 06 日

中 文 摘 要 ： 本研究以表面電漿活化接合(surface activated bonding, SAB)技術運用於金凸塊與銅電極之覆晶接合製程，此活化技術選用物理性氬氣電漿對接合材料表面進行活化處理，期以電漿活化技術降低材料表面之汙染物，進而提高金凸塊與銅電極之熱壓覆晶接合強度。本實驗將試片概分為四種，分別為金凸塊與銅電極均未受氬氣電漿活化處理、金凸塊施予氬氣電漿活化處理，但銅電極未受氬氣電漿活化處理、金凸塊未施予活化處理，但銅電極進行活化處理、金凸塊與銅電極均受氬氣電漿活化處理。試片隨後於於大氣下，金凸塊熱壓覆晶接合於銅電極，以剪力測試量測金凸塊與銅電極之接合強度，並進行橫截面與破斷面之觀察。實驗結果顯示銅電極與金凸塊均經電漿活化之熱壓覆晶接合試片，其剪力值為四者最高，其次為銅電極受氬氣電漿活化處理，但金凸塊未受活化處理之試片，而剪力值最低之試片為金凸塊與銅電極均為受氬氣電漿活化處理。由金凸塊與銅電極之接合介面觀察得知金凸塊與銅電極均經氬氣電漿活化處理者，其接合介面最為完整，無脫層(delamination)或裂縫等缺陷，經氬氣電漿活化處理後之銅電極表面由歐傑電子儀之表面分析結果得知表面之碳含量下降，且接觸角變小，證實氬氣電漿活化處理可有效降低銅電極與金凸塊表面之污染物，進而提高金凸塊與銅電極之熱壓覆晶接合強度。此實驗結果亦驗證電漿活化技術運用於大氣下，熱壓覆晶接合金凸塊與銅電極之可行性。

中文關鍵詞： 電漿活化接合、熱壓覆晶接合、金凸塊、銅電極

英 文 摘 要 ： The plasma surface activated bonding (SAB) technique was applied in flip chip bonding of chips and substrates. An argon gas was selected to perform the physical plasma treatment on the bonding surface of gold bumps and copper electrodes. The plasma-activated technology was expected to reduce the surface contaminants and oxides and to improve the bonding strength of chips and substrates. The experimental results presented an effective improvement of the die-shear force performance of gold bumps and copper electrodes assembly using argon plasma activation. The improvement of the die-shear force was attributed to a better bonding surface of gold bumps and copper electrodes obtained owing to the containments on the surface of the bonding materials was removed by the argon plasma. For gold

bumps and copper electrodes were activated by argon plasma, neither delamination nor crack is found at bonding interface between gold bumps and copper electrodes. A low contact angle was also determined on the surface of copper electrodes after argon plasma activated, indicating a clean bonding surface was achieved. Furthermore, the deposited layers of the copper electrode were pulled away by the gold bump after the die-shear test, and a concavity was formed on the surface of copper electrodes. This experimental result indicates that bonding strength of gold bumps and copper electrodes assembly even higher than the adhesive strength between the deposited layers of copper electrodes. A clear atomic interdiffusion between gold bumps and copper electrodes was observed for specimens were subjected to argon plasma activation. The argon plasma activation was an effective scheme to improve the bonding strength of the assembly of chips and substrates. Thus, the argon plasma activation has great potential to be applied to chips and substrates assembly using thermal compression bonding process.

英文關鍵詞： argon plasma activation, thermal compression bonding, copper electrode, gold bump.

以表面活化接合技術開發晶片與基板之室溫覆晶接合製程與其接合機理之研究

Study on the bonding mechanism and process development for the assembly of chips and substrates at room temperature using surface activated bonding technique

計畫編號：NSC-100-2221-E-040-008
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計畫主持人：莊正利　　中山醫學大學 教授

一、中文摘要

本研究以表面電漿活化接合(surface activated bonding, SAB)**技術運用於金凸塊與銅電極之覆晶接合製程，此活化技術選用物理性氬氣電漿對接合材料表面進行活化處理，期以電漿活化技術降低材料表面之汙染物，進而提高金凸塊與銅電極之熱壓覆晶接合強度。本實驗將試片概分為四種，分別為金凸塊與銅電極均未受氬氣電漿活化處理、金凸塊施予氬氣電漿活化處理，但銅電極未受氬氣電漿活化處理、金凸塊未施予活化處理，但銅電極進行活化處理、金凸塊與銅電極均受氬氣電漿活化處理。試片隨後於於大氣下，金凸塊熱壓覆晶接合於銅電極，以剪力測試量測金凸塊與銅電極之接合強度，並進行橫截面與破斷面之觀察。實驗結果顯示銅電極與金凸塊均經電漿活化之熱壓覆晶接合試片，其剪力值為四者最高，其次為銅電極受氬氣電漿活化處理，但金凸塊未受活化處理之試片，而剪力值最低之試片為金凸塊與銅電極均為受氬氣電漿活化處理。由金凸塊與銅電極之接合介面觀察得知金凸塊與銅電極均經氬氣電漿活化處理者，其接合介面最為完整，無脫層**(delamination)**或裂縫等缺陷，經氬氣電漿活化處理後之銅電極表面由歐傑電子儀之表面分析結果得知表面之碳含量下降，且接觸角變小，證實氬氣電漿活化處理可有效降低銅電極與金凸塊表面之污染物，進而提高金凸塊與銅電極之熱壓覆晶接合強度。此實驗結果亦驗證電漿活化技術運用於大氣下，熱壓覆晶接合金凸塊與銅電極之可行性。**

關鍵詞: 電漿活化接合、熱壓覆晶接合、金凸塊、銅電極

二、英文摘要

The plasma surface activated bonding (SAB) technique was applied in flip chip bonding of chips and substrates. An argon gas was selected to perform the physical plasma treatment on the bonding surface of gold bumps and copper electrodes. The plasma-activated technology was expected to reduce the surface contaminants and oxides and to improve the bonding strength of chips and substrates. The experimental results presented an effective improvement of the die-shear force performance of gold bumps and copper electrodes assembly using argon plasma activation. The improvement of the die-shear force was attributed to a better bonding surface of gold bumps and copper electrodes obtained owing to the containments on the surface of the bonding materials was removed by the argon plasma. For gold bumps and copper electrodes were activated by argon plasma, neither delamination nor crack is found at bonding interface between gold bumps and copper electrodes. A low contact angle was also determined on the surface of copper electrodes after argon plasma activated, indicating a clean bonding surface was achieved. Furthermore, the deposited layers of the copper electrode were pulled away by the gold bump after the die-shear test, and a concavity was formed on the surface of copper electrodes. This experimental result indicates that bonding strength of gold bumps and copper electrodes assembly even higher than the adhesive strength between the deposited layers of copper electrodes. A clear atomic interdiffusion between gold bumps and copper electrodes was observed for specimens were subjected to

argon plasma activation. The argon plasma activation was an effective scheme to improve the bonding strength of the assembly of chips and substrates. Thus, the argon plasma activation has great potential to be applied to chips and substrates assembly using thermal compression bonding process.
Keywords: argon plasma activation, thermal compression bonding, copper electrode, gold bump.

三、文獻回顧

矽晶片與基板之覆晶接合製程依其接合能量，可區分為熱壓接合(thermal compression bonding) [1]、超音波接合(ultrasonic bonding) [2]與熱音波接合(thermosonic bonding) [3]，熱壓接合之關鍵參數為下壓力與載台加熱溫度，下壓力可使接合之凸塊與基板電極緊密接觸，而加熱載台之高溫可使接合介面原子相互擴散而鍵結，但矽晶片屬脆性材料，無法承受過大下壓力，因此為提高接合強度，需大幅提高接合溫度，而部分電子元件無法承受過高之加熱溫度，故此接合技術已為超音波接合技術所取代；超音波接合技術於接合過程中，以超音波功率使接合介面之材料相互摩擦，該摩擦熱可提升接合介面溫度與提高接合介面材料之差排密度(dislocation density)，進而軟化接合介面材料，使接合面產生塑性變形(plastic deformation)而接合，超音波接合之關鍵因子為輸入之超音波功率與下壓力，但從過去文獻[4]證實過大超音波功率，易造成晶片銲墊下方(特別是化合物晶片)產生彈坑孔(crater)缺陷，致使凸塊從晶片上脫離，造成封裝後電訊通路之失效(failure)，故此一技術亦逐漸為熱音波覆晶接合技術所取代。

目前電子構裝之覆晶接合製程大部分採用熱音波能量，在覆晶接合過程中，需藉由載台之加熱溫度與超音波功率之輔助，方可完成載板與基板之接合。然而對於溫度敏感之半導體元件或泛用於消費性電子產品之軟性基板等，均無法以較高加熱溫度完成載板與基板之接合，然而為了降低製程溫度，而使用較高之超音波功率進行製程接合，但若引入過高超音波功率易使載板下方產生彈坑孔之脫層[4]，顯然熱音波覆晶接合製程仍有其應用之限制。

現今廣泛使用的氣體電漿大致可分為物理性活化(Physical etching)[5]與反應性活化(Reactive etching)[6]兩大機制，物理性活化主要是以惰性氣體在低壓的狀態下，使用高頻電壓來激發，使惰性氣體變為離子狀態，該離子以高速運動撞擊材料表面，同時將材料表面之氧化膜或污染物清除，達到清潔材料表面之功能。反應性活化通常應用於材料表面之有機物之活化，電漿氣體選用氧氣、氫氣或兩者與惰性氣體之混合氣體，氧離子可與碳-氫有機物反應形成二氧化碳與水，而該反應物可被抽氣系統排至大氣環境，其化學反應式為[7]：CxHyOz + (O*2,O) → CO2 + H2O。選擇電漿活化氣體對材料表面污染物之清潔效果影響很大，所以必須依材料特性與污染物種類，選擇適當之電漿活化氣體。

表面活化接合技術廣泛被運用於微機電系統(MEMS) 晶圓之接合，因晶圓屬陶瓷材料，其熔點相對較高，欲使其產生擴散接合(diffusion bonding)之製程溫度通常超過1000°C[8]，高溫接合環境下，易使接合晶圓產生熱損傷或接合後之殘留熱應力，因此以電漿活化接合技術輔助晶圓之接合便因應而生，其原理為氣體離子經高壓電加速後，電漿離子高速運動活化欲接合材料之表面[9]，具高動能之離子束撞擊欲接合材料表面，可移除材料表面之污染物與氧化層，有效降低欲接合材料表面能障，隨後於適度的加壓製程中使材料接合。Li[10]以氬氣電漿活化表面鍍著銀膜之銅導線架，該研究結果顯示經氬離子電漿活化處理後，鍍著銀層與未鍍銀膜裸銅導線架，表面之接觸角均下降，但短時間、小功率之電漿活化處理，效果並不顯著；反之經長時間、高功率之電漿活化處理後，銅導線架表面之接觸角大幅下降，且表面粗糙度亦較未活化處理小，證實經電漿活化後，可移除材料表面大部分之污染物，活化後材料表面經元素分析，材料表面之碳原子濃度大幅下降，但氧原子之濃度反而上升，結果顯示以氬氣作為電漿活化氣體，無法順利宜除材料表面之氧化膜，故選擇適當之電漿氣體極為重要。Howlader等人[11]將電漿活化接合技術應用於金屬層與軟板接合，金屬層之材料為銅箔，軟板材料為LCP(liquid

crystal polymer)，首先以氬氣電漿清潔欲接合之軟板與銅箔表面，隨後於軟板表面濺鍍一層銅膜，濺鍍銅膜之目的在於提升軟板材料與銅箔之接合強度，隨後於室溫與真空環境中，以滾輪成功壓合銅箔與軟板，該方法解決過去軟板材料與銅箔採用雷射銲接之脫層，有效提高材料接合之完整度與降低接合介面之殘留熱應力。Kim等人[12]以電漿活化接合技術應用於矽晶圓表面鍍著銅膜之接合，製程選用氬氣作為接合表面之活化電漿，於真空、室溫環境下進行接合，實驗結果顯示未經氬氣電漿活化銅膜之主要污染元素為碳與氧，而經氬氣電漿活化60 秒後，可得到潔淨表面，且經氬氣電漿活化60 秒後，銅膜表面粗糙度之變異性不大，分別為1.85nm 與1.78nm，接合後之介面完整無脫層且為銅與銅之接合，未發現中間層的存在，室溫環境下之接合機制為銅原子間吸引力之交互作用，而形成介面原子重新排列接合。Shigetou等人[13]同樣將電漿活化接合技術應用於矽晶圓表面鍍著銅膜之接合，製程也是選用氬氣作為接合表面之活化電漿，於真空、室溫環境下進行接合，然而銅膜經氬氣電漿活化後，放置於不同真空度之艙體中進行室溫之接合，銅膜之接合面積與艙體之真空度成正比，若真空度維持在0.001Pa以上，銅膜之接合面積約為100%，反之若艙體之真空度下降至0.01Pa，銅膜即無法接合，使用化學分析儀檢測無法接合之銅膜表面，該表面已氧化且為連續性成長之氧化銅膜，受氧化銅膜之影響而無法接合，該研究結果顯示易氧化之材料，維持接著表面之潔淨度極為重要，且真空艙之真空度亦為表面活化接合技術之重要因子。

本研究擬以表面活化技術應用於熱壓覆晶製程進行金凸塊與銅電極之接合，並分析接合介面之微觀組織與剪力試驗後之破斷模式，綜整實驗結果，評估電漿活化技術於大氣下，熱壓覆晶接合金凸塊與銅電極之可行性。

四、實驗方法

選用氧化鋁陶瓷基板為承載金凸塊之基板，以網板印刷方式於基板上製作金銲墊，隨後熱音波製程於金銲墊上植金凸塊，每一氧化鋁載板上銲著9個面積陣列之金凸塊，並將植金凸塊之氧化鋁載板切割為尺寸0.96(W)x1.58(L)x0.5(H)mm^3，如圖一所示。隨後以濺鍍法於氧化鋁基板上沈積厚度各為0.1μm之鈦膜與銅膜，後續以電鍍法沈積銅電極各層金屬鍍膜，由於銅電極在大氣之下易產生有氧化，因此在銅電極上表面需鍍著抗氧化性較佳之銀膜，而銀膜與銅膜間易產生交互擴散，故於銀膜與銅膜間鍍著鎳膜作為銅與銀間之擴散阻絕層，基板銅電極鍍膜種類與厚度由外部至內部分別為Ag(0.5μm)/ Ni(0.5μm)/Cu(1.2μm)/ Ti(0.1μm)，

選用氬氣電漿為金凸塊與銅電極之活化電漿，操作參數：功率400 W，底壓140 mTorr、氣體流量 20 sccm，試片之組合概分為四項分別為金凸塊與銅電極均未受氬氣電漿活化處理、金凸塊施予氬氣電漿活化處理，但銅電極未受氬氣電漿活化處理、金凸塊未施予活化處理，但銅電極進行活化處理、金凸塊與銅電極均受氬氣電漿活化處理。銅電極經電漿活化時間參數為0s、10s、30s、60s、90s，金凸塊經電漿活化30s。金凸塊以熱壓覆晶製程接著於銅電極，主要熱壓參數為加壓負荷0.4 kgf、加熱溫度200°C與持溫時間10min。金凸塊熱壓覆晶接著於銅電極後，以剪力試驗(die-shear test)量測其接合剪力值，並以電子顯微鏡(SEM)觀察接合介面之微觀組織與剪力試驗後之破斷面，搭配能量光譜儀(EDS)分析破斷之元素組成，判斷其破斷模式。以歐傑電子儀(Auger spectrometer)分析未經活化處理與活化處理後之金凸塊與銅電極試片，並搭配接觸角之量測，用以驗證氬氣電漿活化處理之成效。綜整實驗結果，評估氬氣電漿活化技術應用於金凸塊與銅電極熱壓覆晶接合之可行性。

五、結果與討論

1. 熱壓覆晶參數之選用

將氧化鋁載板之金凸塊以熱壓覆晶製程接合於基板之銅電極上，固定接合溫度(bonding temperature)為 200°C，接合時間(bonding time)為 30 分鐘，改變接合負荷(bonding load)從 2 kgf 至 10 kgf，金凸塊與銅電極熱壓接合後，使用剪力推力機作進行剪力強度之試驗，並配合金凸塊與銅電極接合

截面之觀察，選定金凸塊與銅電極適合之熱壓覆晶參數。剪力測試所得之平均剪力值係由每一接合負荷取 10 組數值所得之平均值，接合負荷與平均剪力值之關係如圖二所示，顯示平均剪力值隨著接合負荷的增加而提高。圖三為金凸塊與銅電極於不同接合負荷下之橫截面，隨接合負荷之增加，金凸塊接合後之塑性變形(plastic deformation)隨之上升，金凸塊之接合直徑亦隨之增加。圖三(a)為熱壓接合負荷 2 kgf 之接合橫截面，其接著直徑約為 37-47μm，接合後金凸塊之直徑與未進行熱壓覆晶接合之金凸塊直徑差異不大，顯示在此接合負荷下，金凸塊與基板銅電極之接合面積較小，亦說明在此接合負荷下，其平均剪力值較小，如圖二所示；圖三(b)為接合負荷 4 kgf 之接合橫截面，其接著直徑約為 70-80μm，且接合後金凸塊整體之變形呈香菇頭之形狀；圖三(c)為接合負荷 6 kgf 之接合橫截面，其接著直徑約為 85-100μm，接合後之外型已呈現扁平之圓柱狀；圖三(d)為熱壓接合負荷 8 kgf 之接合橫截面，其接著直徑約為 119-130μm，由接合試片之橫截面觀察得知接合負荷為 6－10 kgf 之接著面積都相對較大，雖然剪力值亦呈現較高之趨勢，但接合面積越大之金凸塊因晶片與基板之高度相對較小，不利於後續封膠(under-fill)之作業，且較大之金凸塊接合面積無法滿足電子構裝細間距(fine pitch)之發展趨勢；而接合負荷 2 kgf 之剪力值太小，故本研究使用之接合負荷為 4 kgf。

2. 電漿活化對熱壓接合剪力值之影響

圖四為金凸塊與銅電極接合後，經剪力試驗所得之剪力值，圖中每一平均值係包含 10 組剪力測試之平均值。金凸塊與銅電極均未經氬氣電漿活化處理試片，其覆晶接合後之平均剪力值為 222.6 gf，若將金凸塊施予 30s 之氬氣電漿活處理；而銅電極不進行活化處理，則該試片之覆晶接合平均剪力值上升至 263.9 gf；如果金凸塊不施予活化處理，而銅電極進行 10s 之活化處理，則該組試片之覆晶接合平均剪力值些微上升至 282.8 gf；對金凸塊氬氣活化處理 30s 且銅電極活化 10s，則該組試片之覆晶接合平均剪力值為 342.1 gf，隨銅電極氬氣電漿活化時間增加至 30s，金凸塊與銅電極之覆晶接合平均剪力值達到最大值 347.1 gf，若繼續延長銅電極之氬氣電漿活化時間(30s、60s、90s)，金凸塊與銅電極之覆晶接合平均剪力值僅些微變化，該微小變動應是實驗量測誤差所致，推論氬氣電漿活化處理於 10s-30s 間即可將銅電極表面之污染物清除。此一實驗結果顯示氬氣電漿活化處理有助於提升金凸塊與銅電極於大氣下熱壓覆晶接合，氬氣電漿活化處理應可有效移除金凸塊與銅電極表面之污染物，進而提高金凸塊與銅電極之熱壓覆晶接合平均剪力值。

為進一步驗證氬氣電漿活化處理有助於提升金凸塊與銅電極之熱壓覆晶接合，以電子顯微鏡觀察金凸塊與銅電極之接合介面，如圖五所示。圖五(a)為金凸塊與銅電極均未氬氣電漿活化處理試片之接合介面，可清楚發現脫層(delamination)缺陷發生於接合介面，而僅金凸塊經氬氣電漿活化處理，而銅電極未施予活化處理之試片，其接合介面亦出現接合不佳之脫層缺陷，如圖五(b)所示；若僅銅電極進行氬氣電漿活化處理 30s，金凸塊為進行活化處理，則該試片之接合介面並未發現脫層或裂縫之缺陷，如圖五(c)所示；若將金凸塊與銅電極均進行 30s 之氬氣電活化處理，則該試片之接合介面非常完整，如圖五(d)所示。此一接合介面觀察結果驗證經氬氣電漿活化處理之試片，其接合介面完整，未發現脫層或裂縫等缺陷，進而有效提升金凸塊與銅電極之接合平均剪力值，此一實驗結果與試片覆晶接合平均剪力值之變化一致。

經剪力測試後，金凸塊與銅電極覆晶接合之破斷處發生於接合強度最低之接合處，因此統計金凸塊與銅電極接合試片之破斷點，有助於判斷金凸塊與銅電極之接合品質，金凸塊與銅電極接合試片經剪力試驗後，主要斷裂點發於金凸塊與氧化鋁載板銲墊間、金凸塊與銅電極之接合介面，若斷裂發生於金凸塊與載板銲墊間，則顯示金凸塊與銅電極之接合強度較高，反之亦然。圖六為金凸塊與銅電極接合試片經剪力試驗後，破裂點之統計圖，明顯可發現若金凸塊未進行氬氣電漿活化處理，僅銅電極進行活化處理，其接合試片經剪力測試後，主要破斷點

發生金凸塊與銅電極間，如圖六(a)所示，反觀若金凸塊與銅電極均經氬氣電漿活化處理，其接合試片經剪力測試後之主要斷裂點發生於金凸塊與載板銲墊間，如圖六(b)所示，顯示金凸塊與銅電極接合強度較佳。

圖七為金凸塊與銅電極均未進行氬氣電漿活化處理，該接合試片經剪力測試後之斷面表面型態，該斷裂點發生於銅電極與金凸塊之接合介面，銅電極表面平整，僅出現金凸塊與銅電極覆晶接合之壓痕(indention)，並未出現接合之痕跡，如圖七(a)所示，金凸塊殘留與氧化鋁載板上，該殘留金凸塊斷面平整且未出現明顯之塑性變形(plastic defor,ation)，如圖七(b)所示，故其接合平均剪力值不佳。由能量光譜儀分析銅電極表面接合區域(point 1)與殘留金凸塊表面(point 2)，前者之主要組成元素為銀，如圖七(c)所示，後者之主要元素為金，如圖七(d)所示，此一分析結果顯示金凸塊與銅電極未經氬氣電漿活化處理，其接合試片經剪力測試之主要破壞模式(fracture mode)為接合介面剝離(peeling-off)，此一結果更進一步驗證其接合品質不佳；若金凸塊經氬氣電漿活化處理，而銅電極未施予活化處理，其接合試片經剪力測試後之斷裂面表面型態如圖八所示，少許物質殘留於銅電極表面，如圖八(a)所示，而殘留於氧化鋁載板之金凸塊斷面呈現部分凹凸表面型態，圖八(b)所示。以能量光譜儀分析銅電極表面之殘留物質(point 1)，其主要成分為金，如圖八(c)所示，而殘留金凸塊表面物質(point 2)亦出現銅電極表面銀膜接著層之訊號，如圖八(d)所示，此一結果顯示金凸塊與銅電極產生部分鍵結，殘留於銅電極之表面物質為金，而部分銅電極之銀膜接著層則轉移至金凸塊表面上，故其接合平均剪力值上升(圖四)；圖九所示為剪力試驗後，銅電極經氬氣電漿活化處理，而金凸塊未經電漿活化處理之接合試片斷面型態圖，銅電極表面出現凹洞(concavity)，如圖九(a)所示，推論該凹洞應是金凸塊與銅電極之鍵結接合處，剪力測試時，銅電極表面之銀膜接著層轉移至金凸塊上，如圖九(b)所示。以電子能量光譜儀檢測銅電極表面凹洞(point 1)之主要成分為銀、鎳、磷，如圖九(c)所示，凹洞形成原因為表面銀膜接著層被拔除，轉移至殘留金凸塊表面之破斷面(point 2)，如圖九(d)所示。實驗結果顯示此一試片之破裂模式為金凸塊拔除(pull-out)銅電極表面之銀膜，亦即顯示金凸塊與銅電極具良好之接合；金凸塊與銅電極均經氬氣電漿活化處理，其接合試片經剪力測試後之破斷表面型態如圖十示，銅電極表面出現凹洞，如圖十(a)所示，且氧化鋁載板上殘留金凸塊之斷面出現凹凸接合痕跡，如圖十(b)所示，顯示經氬氣電漿活化處理之金凸塊與銅電極具良好接合，由能量光譜分析儀分析銅電極凹洞(point 1) 之組成包含銀、銅、鎳，如圖十(c)所示，而氧化鋁載板殘留金凸塊斷面(point 2)之組成元素為金、銀、鎳，如圖十(d)所示，由元素分析結果可推論銅電極鍍膜之銀接著層與鎳層於剪力試驗時，被金凸塊拔離(pull-out)，顯示經氬氣電漿活化處理之金凸塊與銅電極，其試片之接合強度較銅電極鍍膜之接著強度(adhesive strength)高，此一實驗結果充分說明氬氣電漿活化可提升金凸塊與銅電極於大氣下之熱壓覆晶接合強度。

3. 氬氣電漿活化對接合表面組成之影響

以歐傑電子儀分析未經氬氣電漿活化處理之金凸塊與銅電極表面，銅電極表面之元素分別為碳、氧、硫與銀等元素，如圖十一所示；金凸塊表面之組成為碳、氧、硫與金元素，如圖十二所示，此一分析結果顯示金凸塊與銅電極之主要污染物為碳與氧。經不同時間氬氣電漿活化後，銅電極表面之碳含量由未氬氣電漿活化處理前之 24.33 (wt%)降至 11.87(wt%)，顯見氬氣電漿活化處理可有效宜除銅電極表面碳含量，相較氬氣電漿活化處理與未活化處理銅電極試片表面之氧含量，分別為 2.83 (wt%)微降至 2.63 (wt%)，隨後又上升至 3.14 (wt%)，此一分析結果顯示氬氣電漿活化處理無法有效移除銅電極表面之氧原子，其原因為氬氣為物理性活化電漿，係以高速之氬原子撞擊銅電極表面而達活化之效能，故無法去除銅電極表面之氧原子。相同分析結果亦出現於金凸塊表面，氬氣電漿可移除金凸塊表面之碳原子，但仍無法移除金凸塊表面之氧原子，如圖十二所示。此實驗結果說明氬氣電漿活化處理提升銅電極與金凸塊覆晶接合平均剪力值之主要

機制為氫氣電漿活化處理可有效表面之碳原子，降低接合材料表面之污染物，進而提升金凸塊與銅電極之熱壓覆晶接合強度，然而氫氣電漿活化處理無法有效移除銅電極與金凸塊表面之氧原子，該氧原子可能對金凸塊與銅電極之熱壓覆晶接合強度產生不良影響，可選用反應式活化電漿(reactive plasma)去除該材料表面之氧原子，此一研究正持續既行中。

接觸角之大小代表材料表面之潤濕性(wettability)，接觸角越大表示材料表面之污染物含量較高，潤濕性較差，易影響材料之接合品質，接觸角為評估材料表面潔淨度之良好指標。為進一步驗證氫氣電漿活化處理對銅電極表面潔淨度之貢獻，對氫氣電漿活化後之銅電極量測其表面接觸角，其結果圖十三所示，未施予電漿活化處理之銅電極其接觸角高達 96.8°，如圖十三(a)所示，而經由電漿活化 10s 之接觸角下降至 51.88°，如圖十三(b)所示，電漿活化處理 30s 和 60s 之接觸角度分別為 57.1° 和 54°，如圖十三(c)、(d)所示，由量測結果顯示經氫氣電漿活化處理後銅電極之接觸角較未處理者大幅下降，然而銅電極之接觸角並未隨電漿活化時間增長而產生大幅下降，推測其原因應為銅電極表面含有部分之氧原子無法去除所致，此一實驗結果與歐傑電子儀之表面分析結果相同。

經電漿活化處理後之銅電極，其接觸角明顯變小，提高銅電極表面之濕潤性，有助於熱壓覆晶過程中金凸塊與銅電極之接合，其覆晶接強度大於熱音波植金凸塊與載板金銲墊間之強度，因此載板銲墊與金凸塊分離之破斷型式增多，如圖六所示，且金凸塊與銅電極接合試片經剪力試驗後之破斷模式為銀膜被金凸塊拔離(pull-out)，並轉移至金凸塊上，進一步驗證氫氣電經活化處理有助於金凸塊與銅電極之接合，待接合表面兩側都經電漿活化之熱壓覆晶試片，其覆晶接合剪力值均比僅任意一側經電漿活化或兩側都未經電漿活化處理之熱壓覆晶接合試片為佳，驗證氫氣電漿活化有助於熱壓覆晶強度之提升。

4. 氫氣電漿活化對接合介面之影響

為進一步探討氫氣電漿活化處理對金凸塊與銅電極覆晶接合之影響，以歐傑電子儀分析金凸塊與銅電極接合介面原子間之交互擴散(atomic interdiffusion)，圖十四為金凸塊與銅電極均未進行氫氣電漿活化處理之熱壓覆晶接合試片，如選擇接合介面無脫層或裂縫之介面，如圖十四(a)所示，進行組成元素之線掃瞄(line scanning)，如圖十四(b)所示，該原子交互擴散軌跡線可清楚發現金原子與銅電極表面銀原子之交互擴散非常有限，顯示金凸塊與銅電極之接合品質不佳；相較於金凸塊與銅電極均經氫氣電漿活化處理之熱壓覆晶接合試片，其接合介面非常完整，無脫層或裂縫等缺陷，如圖十五(a)所示，且清楚顯示金原子與銅電極表面之銀原子產生明顯之交互擴散，如圖十五(b)所示，此一結果顯示，經氫氣電漿活化處理之試片，其接合品質較佳，因氫氣電漿活化處理可有效移除銅電極與金凸塊接合表面之污染物，降低接合材料間能障，在相同熱壓接合參數下，形成有效之交互擴散，進而提高金凸塊與銅電極之接合強度，此線掃瞄分析結果與破斷面觀察結果相符。綜整原子交互擴散分析結果、橫截面與破斷面之觀察並搭配金凸塊與銅電極接合試片之剪力值，充分證明氫氣電漿活化處理有助提升金凸塊與銅電極之熱壓覆晶接合強度。

六、結論

氫氣電漿活化技術可成功應用於金凸塊與銅電極之熱壓覆晶接合，且接合試片之平均剪力值高於試片未進行氫氣電漿活化處理或者僅有金凸塊或僅銅電極經氫氣電漿活化處理試片。經氫氣電漿活化處理試片之接合介面完整，無脫層或裂縫等缺陷。由剪力測試後之破斷圖得知經氫氣電漿活化處理試片之破斷模式為金凸塊拔離部分銅電極表面鍍膜，顯示金凸塊與銅電極之接合強度較銅電極鍍膜之吸附強度還高，故氫氣電漿活化處理有助提升金凸塊與銅電極之接合強度。

經氫氣電漿活化處理後之銅電極，表面碳含量大幅下降，且銅電極表面之接觸角亦隨之下降，提高銅電極表面之潤濕性，顯見氫氣電漿活化處理有效移除金凸塊與銅電極表面之污染物，提高金凸塊與銅電極之熱壓覆晶接合品質。但隨著電漿活化處理時間增

長，銅電極表面接觸角之變化不大，該結果與試片接合後之平均剪力值變化相符，此實驗結果說明氬氣電漿活化提升金凸塊與銅電極接合之主要機制為移除接合材料表面之碳含量，降低接合材料間之能障，有效提高金原子與銅電極表面銀原子之交互擴散塊，進而提高金凸塊與銅電極之熱壓覆晶接合強度。

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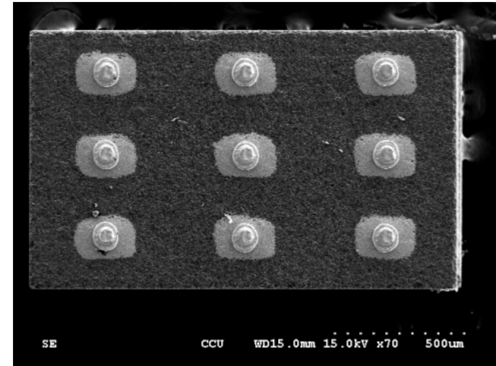
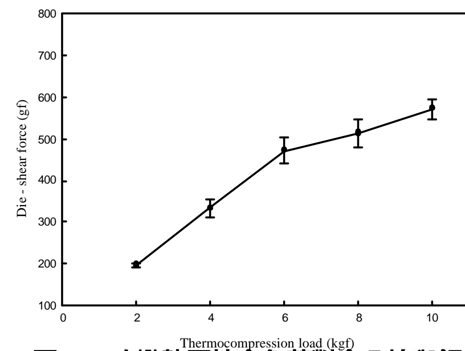
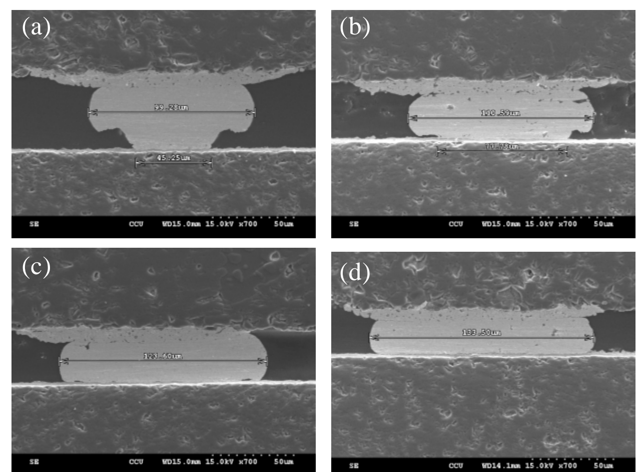
八、圖表



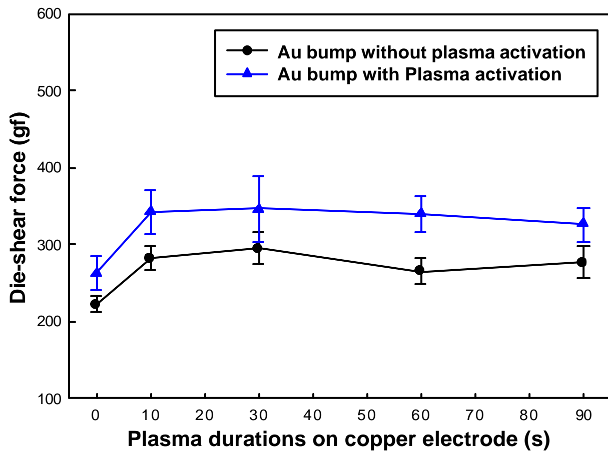
圖一、以熱音波製程於氧化鋁載板上植面積陣列金凸塊



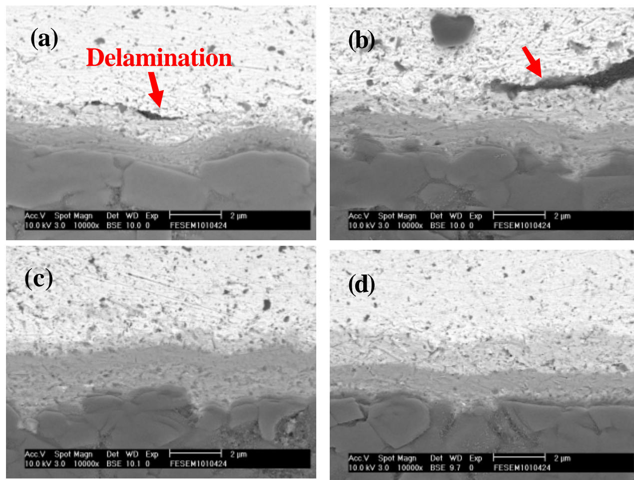
圖二、改變熱壓接合負荷對金凸塊與銅電極接合平均剪力值之影響。



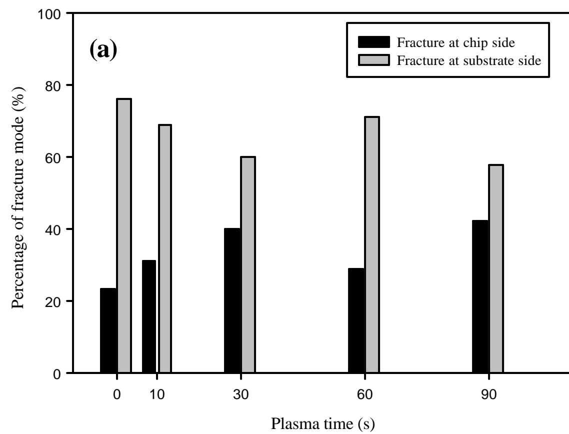
圖三、不同熱壓負荷對金凸塊接著直徑之影響，(a) 2kgf，(b) 4kgf，(c) 6kgf，(d) 8kgf。

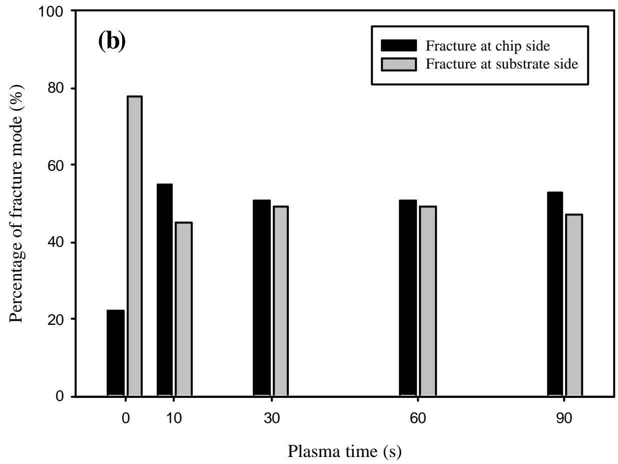


圖四、金凸塊與銅電極經電漿活化與未經電漿活化試片之熱壓覆晶接合平均剪力值

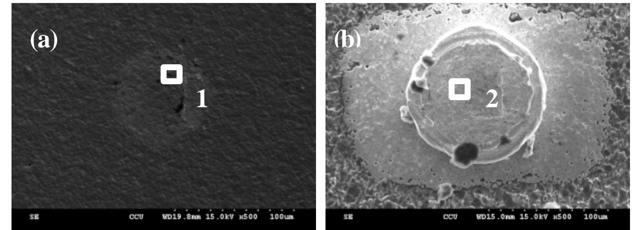


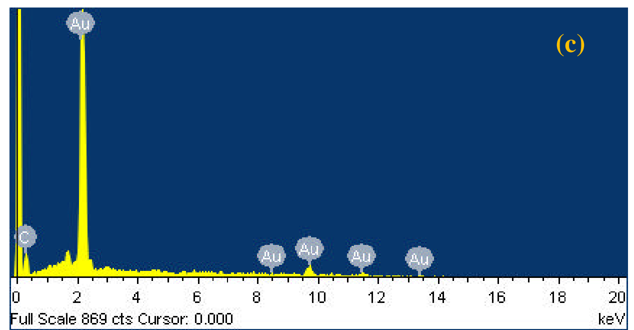
圖五、金凸塊與銅電極經電漿活化與未經電漿活化試片之熱壓覆晶接合介面，(a)金凸塊與銅電極均未進行氬氣電漿活化處理，(b)僅金凸塊進行氬氣電漿活化處理，(c)僅銅電極進行氬氣電漿活化處理，(d)金凸塊與銅電極均經氬氣電漿活化處理。

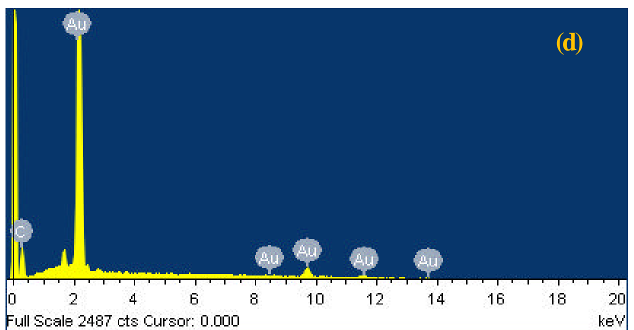




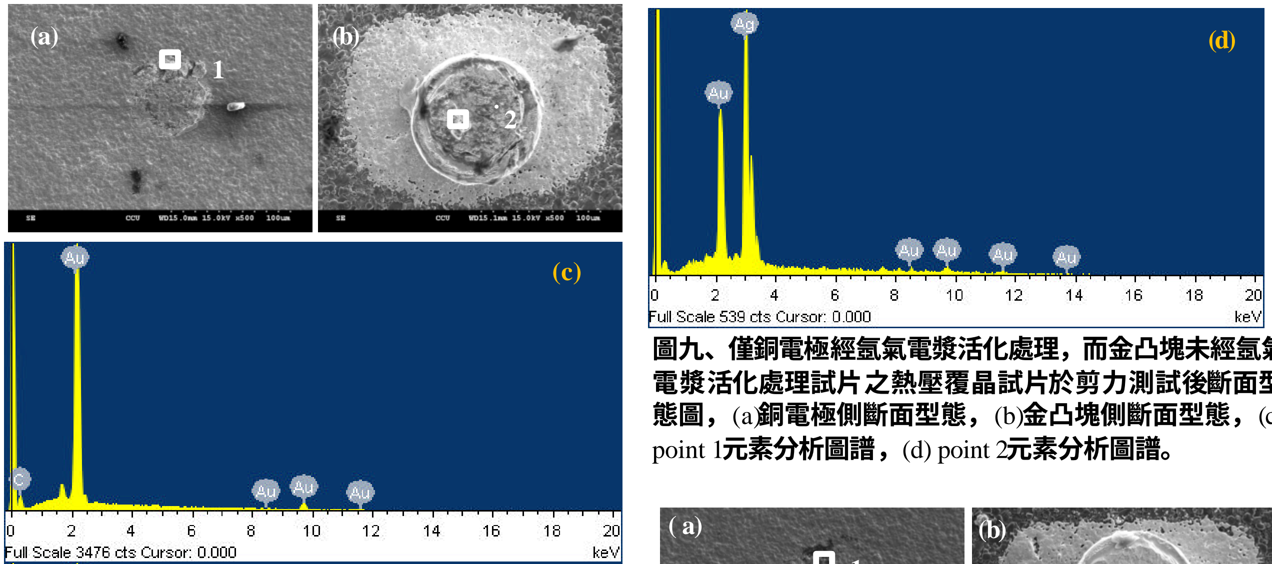
圖六、金凸塊與銅電極經電漿活化與未經電漿活化後，其覆晶接合試片經剪力測試破斷位置統計圖，(a)金凸塊未經表面活化處理，僅銅電極經氬氣電活化處理，(b)金凸塊與銅電極均經氬氣電漿活化處理。

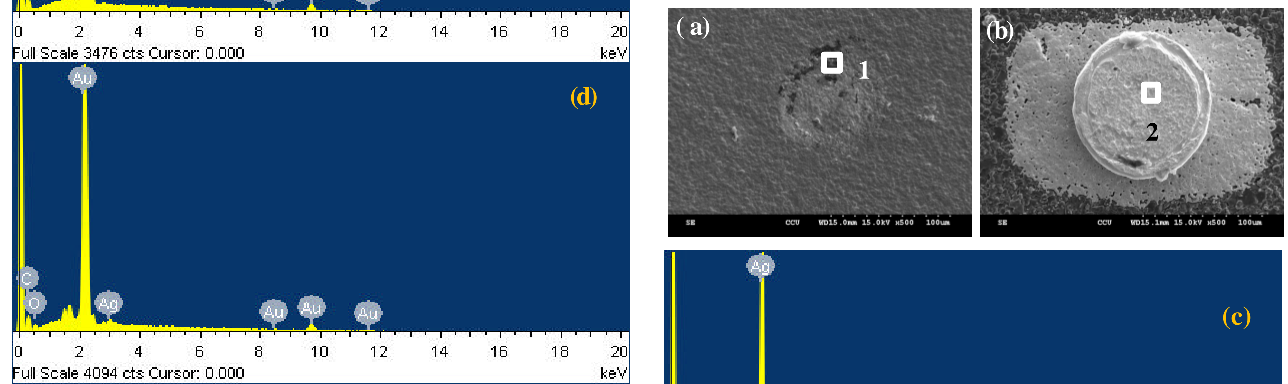






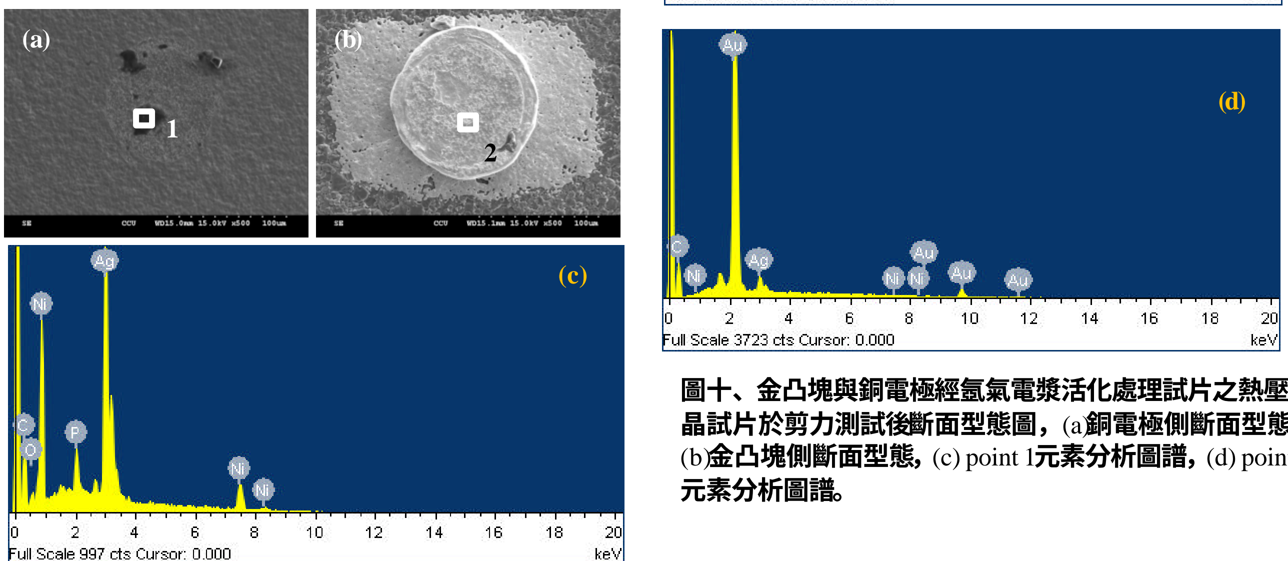
圖七、金凸塊與銅電極未經氬氣電漿活化處理試片之熱壓覆晶試片於剪力測試後斷面型態圖，(a)銅電極側斷面型態，(b)金凸塊側斷面型態，(c) point 元素分析圖譜，(d) point 2元素分析圖譜。



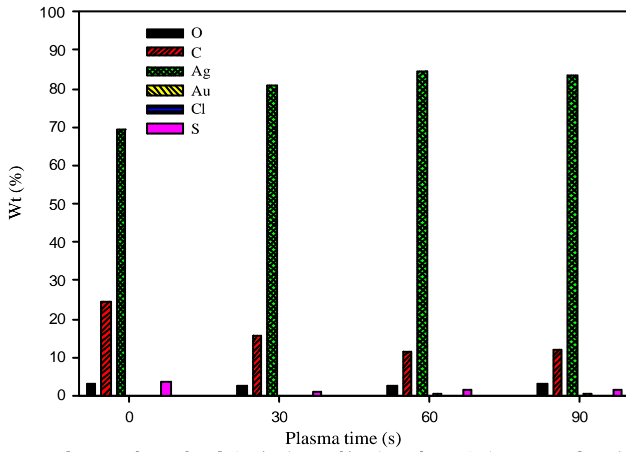


圖八、僅金凸塊經氬氣電漿活化處理，而銅電極未經氬氣電漿活化處理試片之熱壓覆晶試片於剪力測試後斷面型態圖，(a)銅電極側斷面型態，(b)金凸塊側斷面型態，(c) point 1元素分析圖譜，(d) point 2元素分析圖譜。

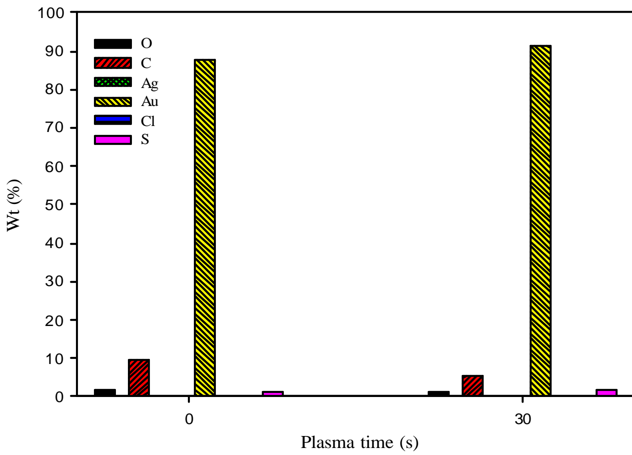
圖九、僅銅電極經氬氣電漿活化處理，而金凸塊未經氬氣電漿活化處理試片之熱壓覆晶試片於剪力測試後斷面型態圖，(a)銅電極側斷面型態，(b)金凸塊側斷面型態，(c) point 1元素分析圖譜，(d) point 2元素分析圖譜。



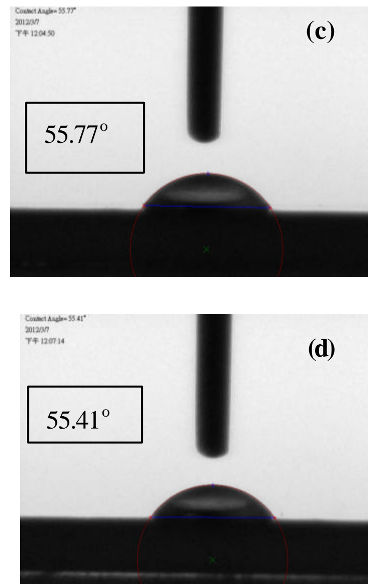
圖十、金凸塊與銅電極經氬氣電漿活化處理試片之熱壓覆晶試片於剪力測試後斷面型態圖，(a)銅電極側斷面型態，(b)金凸塊側斷面型態，(c) point 1元素分析圖譜，(d) point 2元素分析圖譜。



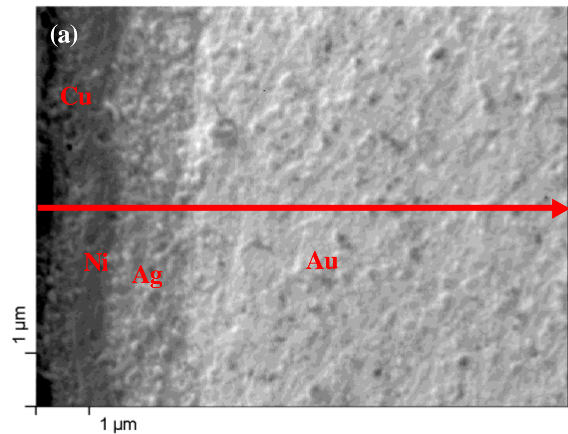
圖十一、銅電極未經氬氣電漿活化處理與經不同時間氬氣電漿活化處理後，銅電極表面元素含量之重量百比。

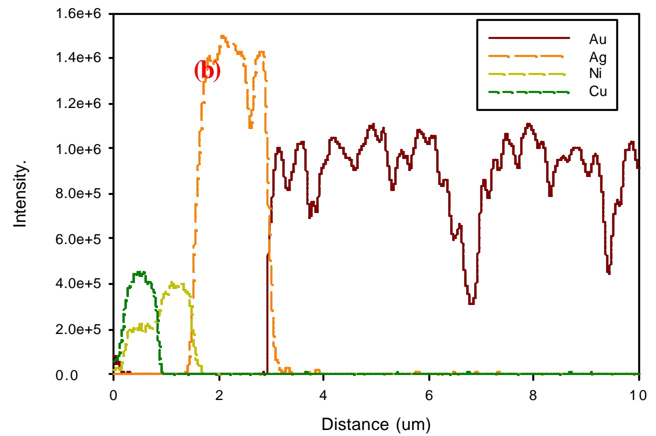


圖十二、金凸塊未經氬氣電漿活化處理與經氬氣電漿活化處理30s後，金凸塊表面元素含量之重量百比。

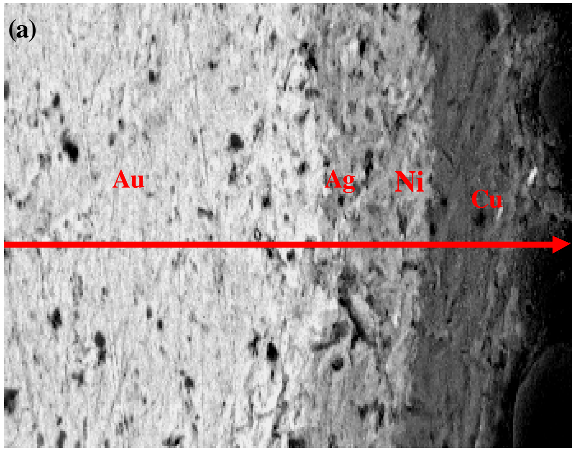


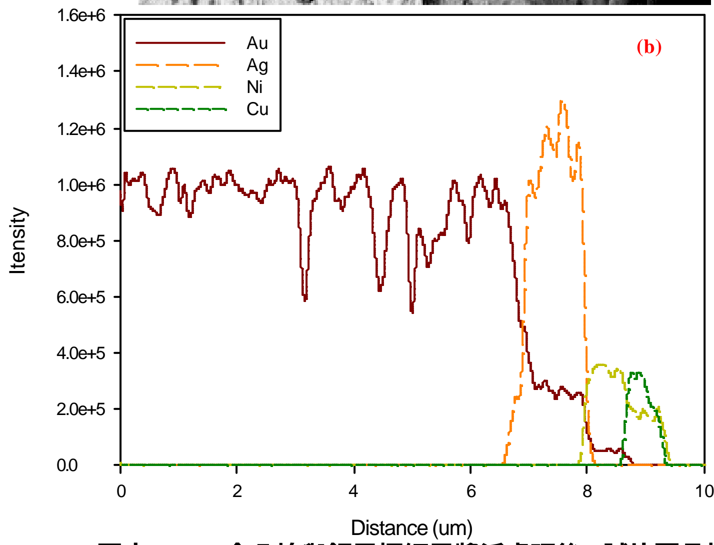
圖十三、銅電極經氬氣電漿活化處理與未經電漿活處理後，銅電極表面之接觸角測試結果，(a)未經氬氣電漿活化(b)電漿活化10s，(c)電漿活化30s，(d)電漿活化60s。





圖十四、(a)金凸塊與銅電極未經電漿活處理，試片覆晶接合介面， (b) 歐傑電子儀線掃描分析。





圖十五、(a)**金凸塊與銅電極經電漿活處理後，試片覆晶接合介面，** (b) **歐傑電子儀線掃描分析。**

國科會補助專題研究計畫出席國際學術會議心得報告

日期：101 年 8 月 30 日

<table>
<tr><td>計畫編號</td><td colspan="3">NSC-100-2221-E-040-008</td></tr>
<tr><td>計畫名稱</td><td colspan="3">以表面活化接合技術開發矽晶片與基板之室溫覆晶接合製程與其接合機理之研究</td></tr>
<tr><td>出國人員姓名</td><td>莊正利</td><td>服務機構及職稱</td><td>中山醫學大學職業安全衛生學系 教授</td></tr>
<tr><td>會議時間</td><td>2012 年 8 月 13 日至 2012 年 8 月 16 日</td><td>會議地點</td><td>Guilin, China</td></tr>
<tr><td>會議名稱</td><td colspan="3">(中文)2012 微電子構裝與高密度封裝國際會議
(英文)2012 International Conference on Electronic Packaging Technology & High Density Packaging</td></tr>
<tr><td>發表題目</td><td colspan="3">(中文)矽晶片以熱音波覆晶接合製程接著於軟性基板之高溫儲存與高濕/高溫可靠度測試研究
(英文) Reliability of HTS and HH/HT Tests Performed in Chips and Flex Substrates Assembled By a Thermosonic Flip-Chip Bonding Process</td></tr>
</table>

一、參加會議經過：

此一電子構裝國際學術會議為目前國際較大型之電子構裝會議之一，由大陸半導體協會主辦，並由中國大陸各重點大學承辦，在中國大陸已有 13 年之久，每年均吸引大量國際電子構裝之研究學者參與此一會議，每年會議時間約在 8 月中旬，今年會議時間為 8 月 13 日至 16 日共 4 日。今年會議議程與主題和過往相符，會議第一天安排短期訓練課程，邀請電子構裝領域著名學者與各微電子構裝公司研發部人員講授電子構裝之各項議題，另舉辦 ASE、3MTS 等公司對半導體封裝技術未來發展趨勢之討論會(ITRS workshop)，該討論內容涵蓋微電子構裝之發展趨勢、材料之應用、生產技術之提升與可靠度相關驗證等。今年會議主題與往年大致相同，可分為八大項：Advanced Packaging & System Integration、Packaging Materials & Process、 Packaging Design and Modeling、High Density & SMT、Advanced Manufacturing & Packaging Equipment、Quality & Reliability、Solid State Light Packaging and Integration、Emerging Technologies。隨電子構裝技術之成熟化與大量半導體廠商西進大陸，台灣主要之電子構裝廠商亦前往中國大陸設廠，因此，在會議中可見來自台灣的贊助廠商或台灣構裝業者至中國大陸設廠之研發人員與技術人員，中國大陸的廠商亦高度投入此次會議，可見微電子構裝技術在中國大陸的蓬勃發展。

二、與會心得：

主辦單位將議程第二天安排微電子構裝技術各領域專家進行專題演講，包括知名封裝學者 Prof. R. R. Tummala、Prof. Johan Liu、Dr. Wolf Jurgen、Dr. Viorel Dragol 等，其中 Prof. Johan Liu 提出晶片與基板接合之導電膠膜(conductive film)，該膠膜之設計要點要過去泛用之導電膠相似，以熱塑性高分子(ploymer)與導電顆粒(conductive particle)所構成，

但隨晶片堆疊(stack)**之需求提高，單位晶片厚度大幅下降且模組之晶片數目增多，散熱已成模組之重要課題，故於導電膠膜中添加高導熱係數之碳化矽**(SiC)**，提高膠膜之導熱性，該導電膠膜經固化**(cured)**後之剪力強度**(shear strength)**可達** 6.5 MPa**，導熱能力達** 0.37 W/mk**。筆者會議中亦提出導電膠膜之發展過程中，添加導電顆粒之數量對晶片凸塊與基板電極之接合電阻產生嚴重影響, 若考慮以非導膠膜添加碳化顆粒作為晶片與基板接合膠膜，亦可提高晶片基板之散熱能力，此一選擇是否優於導電膠膜之選擇？**Prof. Johan Liu **表示此為一項優異之選擇且深應發展潛力。**Dr. Wolf Jurgen **則針對** 3D **堆疊技術做完整介紹，包括材料選擇、製程運用與後續因應力所產生之可靠度問題。、**Dr. Viorel Drago **則介紹** wafer to wafer **與** chip to wafer **技術，該接合技術之製程溫度需低於** 400**℃，顯然很多輔助能量(如超音波等**…)**需被加入方可達成接合之目的，該演講中特別指出接合介面之乾淨度是影響接合品質之重要因素，故提出適合之清潔溶液**(cleaning solution)**，該清潔容液可有效移除晶圓接合表面之污染物，進而提高晶圓與晶圓之接合強度。日本** Suga **教授則運用過去提出「自我活化接合(Self activated bonding ;SAB)」技術應用於晶片之** 3D **堆疊，並於接合表面直入鐵原子，使接合製程得以在大氣下進行。顯見此次會議之主題以晶片之** 3D **堆疊、晶圓層級之高等封裝技術為主。**

三、發表論文全文或摘要：

Abstract

This study assesses the reliability of the high-temperature storage (HTS) test and high humidity/high temperature (HH/HT) test for an assembly of chips thermosonically bonded onto flex substrates. Environmental parameters used in the HTS and HH/HT tests were consistent with joint electron device engineering council (JEDEC) specifications. The die-shear test was applied to examine changes in die-shear forces for specimens subjected to HTS and HH/HT test. The microstructure of test specimens was analyzed to evaluate reliability and to identify possible failure mechanisms. Die-shear force decreased slightly as HTS test duration increased. When the duration of the HTS test was increased, the percentage of gold bumps that peeled off of the surface of copper pads on the chip side increased, and crack existed at the bonding interface between gold bumps and bond pads of silicon chips. This crack was formed due to thermal stress generated during the HTS test, and degraded the die-shear force of the assembly of chips and flex substrates. Cracks and blisters that occurred at the bonding interface between gold bumps and bond pads of silicon chips after HH/HT tests of varying durations deteriorated the die-shear forces. Blisters that formed on the bond pad surfaces resulted from moisture penetrating the deposited layers of bond pads before being vaporized. The reliability of HTS and HH/HT test must be improved to prevent crack forming at the bonding interface between the gold bumps and bond pads and to prevent moisture from penetrating the deposited layers of bond pads.

Keywords: Thermosonic flip-chip bonding process, HTS test, HH/HT test, flex substrate

全文如下頁所示：

Reliability of HTS and HH/HT Tests Performed in Chips and Flex Substrates Assembled By a Thermosonic Flip-Chip Bonding Process

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Abstract

This study assesses the reliability of the high-temperature storage (HTS) test and high humidity/high temperature (HH/HT) test for an assembly of chips thermosonically bonded onto flex substrates. Environmental parameters used in the HTS and HH/HT tests were consistent with joint electron device engineering council (JEDEC) specifications. The die-shear test was applied to examine changes in die-shear forces for specimens subjected to HTS and HH/HT test. The microstructure of test specimens was analyzed to evaluate reliability and to identify possible failure mechanisms. Die-shear force decreased slightly as HTS test duration increased. When the duration of the HTS test was increased, the percentage of gold bumps that peeled off of the surface of copper pads on the chip side increased, and crack existed at the bonding interface between gold bumps and bond pads of silicon chips. This crack was formed due to thermal stress generated during the HTS test, and degraded the die-shear force of the assembly of chips and flex substrates. Cracks and blisters that occurred at the bonding interface between gold bumps and bond pads of silicon chips after HH/HT tests of varying durations deteriorated the die-shear forces. Blisters that formed on the bond pad surfaces resulted from moisture penetrating the deposited layers of bond pads before being vaporized. The reliability of HTS and HH/HT test must be improved to prevent crack forming at the bonding interface between the gold bumps and bond pads and to prevent moisture from penetrating the deposited layers of bond pads.

Keywords: Thermosonic flip-chip bonding process, HTS test, HH/HT test, flex substrate

Introduction

Flex substrates are very attractive for use in portable electronic products as they are both light and flexible. Generally, an assembly of chips and flex substrates is fabricated using a flip-chip bonding process with adhesives, including isotropic conductive paste (ICP), anisotropic conductive paste (ACP) and nonconductive paste (NCP) [1-3]. Bonding strength of an assembly of chips and flex substrates is mainly the cured strength of the adhesive. To achieve sufficient bonding strength, curing temperature and curing time must be controlled precisely. This increases manufacturing cost of electronic packaging. Therefore, this work proposes a novel and direct bonding process for the assembly of chips and flex substrates fabricated using the thermosonic flip-chip bonding process [4]. A nickel layer was deposited onto the surface of the copper layer to enhance the rigidity of copper electrodes over flex substrates. Ultrasonic power was then transferred to the bond interface between the gold ball and copper electrode during the thermosonic wire bonding process. Bonding strength and bondability of gold bumps bonded to copper electrodes over flex substrates were thus improved [5].

Several reliability tests for gold wires bonded onto aluminum pads or copper wires bonded onto aluminum pads using the wire bonding process have been investigated [6-8]. Ji *et al.* [6] demonstrated that intermetallic compounds (IMCs) formed and grew as the durations of the thermal aging test increased. Kirkendall voids also developed during thermal aging test due to differences in the atomic diffusion coefficient of Au and Al. As test duration increased, severe Kirkendall voids congregated and formed a crack; this crack ran through the interface of the gold bond and IMC. The failure mechanism of gold balls bonded onto aluminum pads subjected to the HTS test at 175°C for 2000 h was identified [7]. Pull strength decreased as test durations increased from 1500 h to 2000 h, and fracture location at the necking zone of the gold wire was transformed into the fracture mode of the gold ball lifting away from bond pads. The cross section of ball bonds showed that the IMC layer of Au_4Al transformed into new microstructures after the 2000-h HTS test. These new microstructures reduced the adhesive strength between gold balls and bond pads. Pull strength was thus degraded as duration of the HTS test increased. Uno [8] investigated the reliability of the PCT on copper wire thermosonically bonded onto an aluminum pad. The copper wire coated with palladium had better reliability by the PCT than bare copper wire. A continuous crack existed at the bond interface between the bare copper ball and aluminum pad after the 400-h PCT. A uniform IMC layer formed; its thickness was < 0.2 μm when a copper wire coated with palladium was bonded onto the aluminum pad after the 400-h PCT. This thin and uniform IMC layer can improve bond strength between ball bonds and bond pads. However, IMC layer thickness increased as reliability test duration increased, and a crack or voids existed. To reduce the adverse effect of the IMC layer on the reliability of ball bonds, the selection of materials for bond pads and bond wires is critical.

Few studies have investigated the reliability of chips bonded onto flex substrates using the thermosonic flip-chip bonding process. This study verifies the reliability of the HTS and HH/HT tests for chips bonded onto flexible substrates by thermosonic flip-chip bonding. Parameters for reliability tests of the HTS test and PCT were complied based on the JEDEC specifications [9, 10]. After the HTS and HH/HT tests with

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various test durations, the die-shear test was applied to examine changes in die-shear forces and a scanning electron microscope (SEM) was used to observe the microstructure of specimens to evaluate reliability further.

Experimental methods

The thermosonic flip-chip bonding process was utilized to fabricate the flex substrates and chips assemblies. Flip-chip bonding experiments were performed using the automatic thermosonic flip-chip bonder developed by Taiwan's Industrial Technology Research Institute (ITRI). To determine the accuracy of reliability of the HTS and HH/HT tests, bonding quality of the chips and flexible substrates assembly should be controlled within a narrow range. A stable die-shear force of the assembly of chips and flex substrates can be achieved using thermosonic flip-chip bonding parameters of 20.66W ultrasonic power, 0.3 s bonding time, 200°C bonding temperature, and 930 gf bonding load.

The stacking structure of bond pads in this study from top to bottom was Ag/Ti/Cu/Ti/Si. The bumping process parameters for gold stud bumps onto bond pads have been described previously [11]. Silver was deposited onto the surface of bond pads as a bonding layer to improve bond strength and the bondability of gold bumps, which were studded on bond pads of silicon chips. An outer titanium layer was deposited on the copper layer as a diffusion barrier layer to prevent copper atoms diffusing out to the surface of the silver layer from oxidizing during the thermosonic bumping process. A sound bump with sufficient bonding strength was achieved. The inner titanium deposited onto bond pads was expected to improve adhesive strength between the silicon chip and copper film. Each chip had eight gold stud bumps. Deposited layers of copper electrodes over flexible substrates from top to bottom were Ag/Ni/Cu/PI [5]. A nickel layer was deposited on the surface of copper electrodes to enhance copper electrode rigidity and improve bond quality of the assembly of chips and flexible substrates, as described in our previous work [4].

Specimens were then subjected to the HTS and HH/HT tests to assess test reliability. Test durations and parameters were consistent with JEDEC specifications [9, 10] (Table 1). The die-shear test was applied to identify variations in die-shear forces after the HTS and HH/HT tests. An SEM and an energy dispersive spectrometer (EDS) were utilized to verify the fracture mode, examine fracture morphology, determine the compositions at the fracture location, and elucidate the fracture mechanism after the die-shear test. Field-emission Auger electronic spectroscopy (FEAES) was applied to determine the atomic interdiffusion between gold bumps and copper electrodes after the HTS test. The reliability of the HTS and HH/HT tests was evaluated and the fracture mechanism was identified based on experimental and analytical results.

Table 1 Reliability testing parameters for chip thermosonically bonded onto flex substrates [9, 10]

	HTS test	HH/HT test
Test parameters	+150 °C	+85°C,85% RH
Read point (h)	200,400,600,800, 1000	200,400,600,800, 1000

Results and discussion

High-temperature storage test

Die-shear test after the HTS test

Thermosonic flip-chip bonding was used in this study to fabricate assemblies of chips and flexible substrates. The bonding parameters were 20.66W ultrasonic power, 0.3 s bonding time, 200°C bonding temperature, and 930 gf bonding load. After chips were bonded onto flexible substrates, specimens were subjected to the HTS test at 150°C for 1000 h. The effect of the HTS test on bond quality was evaluated by the die-shear test for each test duration of 200 h. Figure 1 shows the relationship of die-shear forces versus HTS test durations. The die-shear force of the assembly of chips and copper electrodes with the nickel layer was higher than that of the assembly of chips and copper electrodes without a nickel layer. The elastic modulus of copper electrodes over flex substrates was increased from 68.7 GPa with no such layer to 108 GPa when a nickel layer was deposited on the copper electrode [5]. Depositing a nickel layer on the copper electrodes effectively improves the rigidity of copper electrodes over flex substrates, increasing the bonding efficiency under ultrasound at the bond interface between the gold bumps and copper electrodes. The die-shear force of the assembly of chips and copper electrodes with the nickel layer was thus enhanced. For the assembly of chips and flex substrates with the nickel layer, die-shear forces did not decrease significantly as HTS test duration increased. Die-shear forces varied in the range of 700-800 gf. A reasonable minimum required die-shear force, based on JEDEC specifications [12], was approximately 547 gf according to the averaged apparent diameter of gold bumps. Obviously, all die-shear forces of assemblies of chips and copper electrodes with the nickel layer were higher than the minimum requirement in JEDEC specifications for test durations of 0-1000 h.

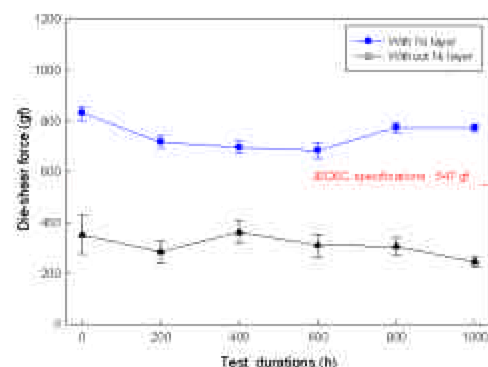


Fig. 1 Relationships between the die-shear forces and test durations of the HTS test for chips and flex substrates assembly.

In contrast to high die-shear forces were obtained for assemblies of chips and copper electrodes with the nickel layer, all die-shear forces of assemblies of chips and copper electrodes without a nickel layer were far lower than 547 gf after the HTS tests with various durations. A weak bond formed between the gold bumps and copper electrodes before the HTS test. Crack occurred at the bonding interface of gold bumps and copper electrodes [4], and atomic interdiffusion did not improve bond quality as HTS test duration increased. Thus, die-shear forces were not enhanced (Fig. 1). The die-shear forces of the chips bonded onto flexi substrates without the nickel layer were far lower than the minimum in the JEDEC specifications for each HTS test duration. Thus, no further experiments and analyses were required after the HTS test for specimens with chips bonded onto flexible substrates without a nickel layer.

To verify possible change at the bond interface after the1000-h HTS test, the cross section of the chips bonded onto copper electrodes with the nickel layer was examined using an SEM. The flexible substrates were deformed and gold bumps were strongly bonded onto copper electrodes over the flexible substrates (Figs. 2a and b). Young's modulus of the flexible substrate was lowest between the gold bump and silicon chip, and the flexible substrate had the greatest flexibility and deformed easily when subjected to the HTS test. Neither delamination nor cracks existed at the bond interface between the gold bumps and copper electrodes. Thus, the gold bumps were firmly bonded onto the flexible substrates after the 1000-h HTS test (Fig. 2b).

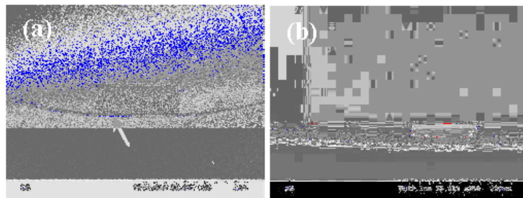
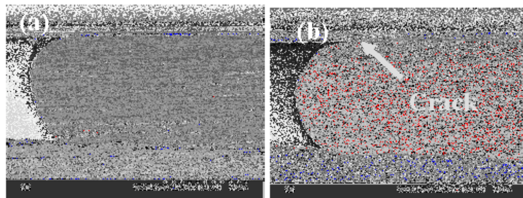


Fig. 2 SEM micrographs of (a) cross section of chip bonded on flex substrate after the 1000-h HTS test, (b) large magnification of cross section of the gold bump bonded on copper electrodes.



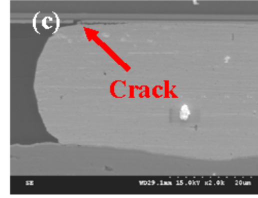


Fig. 3 SEM micrographs of (a) cross section of gold bump bonded on copper electrodes not subjected to the HTS test, (b) cross section of gold bump bonded on copper electrodes after the 400-h HTS test, (c) cross section of gold bump bonded on copper electrodes after the 1000-h HTS test.

Notably, an SEM was used to examine the bond interface between the bond pad of silicon chips and gold bump for specimens not subjected to HTS testing and specimens subjected to the 400-h and 1000-h HTS tests (Figs. 3a-c). A sound bond without delaminations or cracks existed at the bond interface for specimens not subjected to the HTS test (Fig. 3a). When test durations were extended to 400 h and 1000 h, crack occurred at the bond interface between bond pads of silicon chips and gold bumps (Figs. 3b and c). In contrast to the strongly bond between gold bumps and the flexible substrates for specimens not subjected to the HTS test, crack occurred at the bond interface between gold bumps and bond pads of silicon chips due to the thermal stress that was generated during the HTS test. Thermal stress may be due to a mismatch of the thermal expansion coefficient between the silicon chip and gold bumps. This crack reduced die-shear forces after HTS tests of various durations.

Fracture modes analysis after the HTS test

After the die-shear test, fracture modes of specimens were divided into three categories: deposited layers of copper electrodes pulling out by gold bumps; gold bumps peeling off of the surface of copper electrodes; and, gold bump peeling off of the surface of bond pads of silicon chips (Figs. 4a-c). Deposited layers of copper electrodes were pulled away from the bond area by gold bumps, indicating that bond strength between gold bumps and copper electrodes was higher than the adhesive bond between deposited layers. Thus, this fracture mode implies that the die-shear force did not degrade after the HTS test. However, gold bumps peeled away from the surface of bond pads of silicon chips, indicating that defects existed in the bond interface. Die-shear forces can be degraded by defects forming after the HTS test. Similarly, gold bumps peeling off of the surface of copper electrodes also indicate that bond strength between gold bumps and copper electrodes was poor.

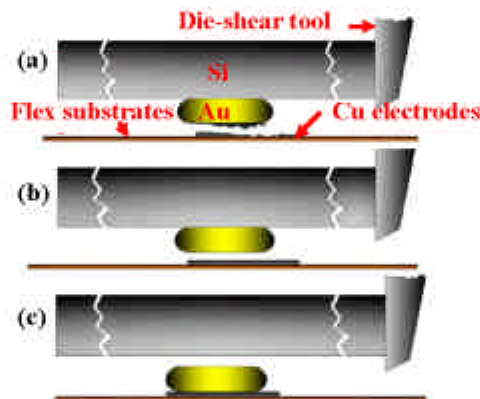


Fig. 4 A sketch to illustrate the fracture modes of chips and flex substrates assembly after the die-shear test, (a) the deposited layers of copper electrodes was pulled-out by gold bumps, (b) gold bumps peeled-off of the surface of copper electrodes, (c) gold bumps peeled-off of the surface of bond pads of silicon chips.

To analyze changes in fracture modes under various HTS test durations, fracture mode of each bump was calculated and plotted (Fig. 5). For specimens not subjected to the HTS test, the main fracture mode was gold bumps pulling away from deposited layers of copper electrodes, and no fracture mode existed for gold bumps peeling off of bond pads of silicon chips. Figure 6 shows fracture morphologies of copper electrodes and gold bumps for specimens not subjected to the HTS test. A portion of the deposited layers of copper electrodes was pulled away and a concavity formed on copper electrodes, and the pulled away layer stuck onto the gold bump (Figs. 6a and b). The EDS was utilized to identify the compositions of the concavity on copper electrodes and the pulled away layer stuck onto the gold bump. Copper was the main component in the concavity and the layer stuck onto the gold bump was composed of nickel and silver. This analytical result implies that a portion of deposited layers was pulled out of the interface between copper and nickel and bond strength of the gold bumps bonded onto copper electrodes was higher than that of the adhesive between deposited layers.

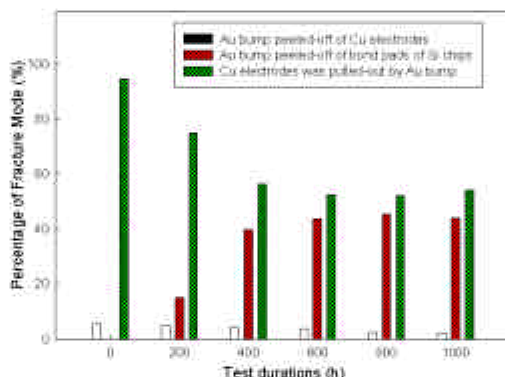


Fig. 5 The percentage of fracture modes for specimens not and subjected the HTS test with various test durations.

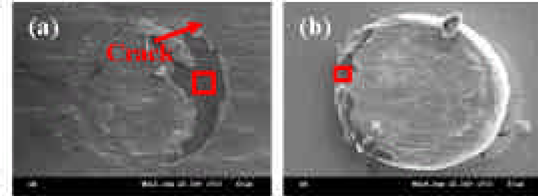


Fig. 6 SEM micrographs of (a) fracture morphology of the copper electrode, (b) fracture morphology of a gold bump. The chips bonded on flex substrates without subjected to the HTS test.

As HTS test duration increased, the percentage of gold bumps peeling off of the surface of bond pads was increased (Fig. 5). This fracture mode was due to crack at the bond interface between gold bumps and bond pads of silicon chips (Fig 3), which degrade die-shear force as HTS test duration increased. This experimental result is consisted with changes in die-shear forces (Fig 1). Figure 7 shows the three fracture mode categories for specimens subjected to the 1000-h HTS test. A crack existed on the fracture morphology of copper electrodes and a deformed gold bump was observed in the fracture morphology of gold bumps (Figs. 7a and b). This fracture mode is similar to that of specimens not subjected to the HTS test (Fig. 6). The crack and deformed gold bump suggest that bond strength of specimens remained good after the HTS test. For the fracture mode of gold bumps peeling off of the surface of copper electrodes, the crack was also observed on the surface of copper electrodes after die-hear test (Fig. 7c) and a deformed gold bump existed on the fracture morphology of the silicon chips (Fig. 7d). As mentioned, this peeling-off fracture mode indicates weak bond strength of specimens after the HTS test; however, the crack existed on the fracture morphology of copper electrodes and a deformed gold bump existed after the die-shear test, suggesting that good bond strength can be obtained with this fracture mode. Figures 7e and f show the gold bump that peeled away from the bond pad of silicon chips. Fig. 7f shows the fracture morphology of bond pads; only a portion of deposited layers was pulled out of the central bond area. The periphery of the bond area appeared a flatten separation between the bond pad and gold bump. These observational results indicate that this fracture mode was enhanced by crack at the interface between bond pads and gold bumps after the HTS test (Fig. 3c). Figure 7e shows a non-deformed gold bump. Figure 3c shows crack at the interface between bond pads and gold bumps, indicating that bond strength was weak with this fracture mode. Thus, die-shear forces decreased as HTS test duration increased.

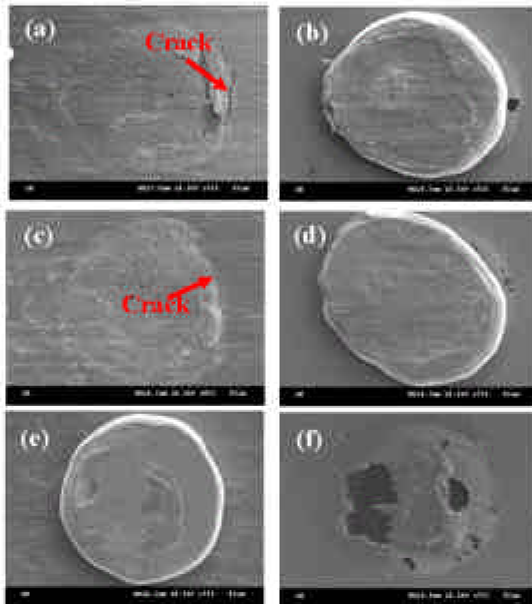
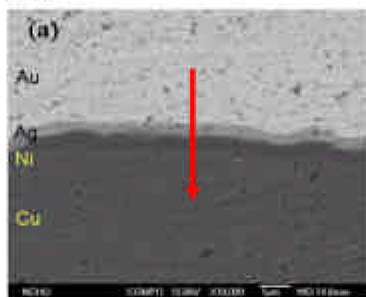


Fig. 7 SEM micrographs of fracture morphology of (a) the copper electrode on flex substrate, (b) the gold bump on the silicon chip, (c) the copper electrode on the flex substrate, (d) the gold bump on silicon chip, (e) the gold bump on silicon chip, (f) bond pad on silicon chip. The specimens were ubjected to the 1000-h HTS test.

Line scanning by FEAES was conducted to identify the atomic interdiffusion between the gold bump and copper electrodes. A sound bond was achieved and no crack or voids were observed at the bond interface between gold bumps and copper electrodes after the 1000-h HTS test (Fig. 8a). The obvious atomic interdiffusion between the gold bump and silver layer was obtained for specimens subjected to the 1000-h HTS test. Atomic interdiffusion effectively enhances bond strength. Hence, the reliability of the HTS test for the gold bumps and copper electrodes assembly should not be an important issue.



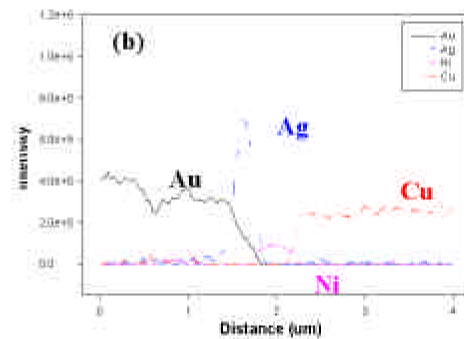


Fig. 8 (a) The cross-section of Au bump bonded on copper electrode after the 1000-h HTS test, (b) line scanning profile of the bond interface between gold bump and copper electrode after the 1000-h HTS test.

The reliability of the HTS test demonstrates that a sound bond can be achieved between gold bumps and copper electrodes. However, thermal stress formed at the interface between gold bumps and bond pads of silicon chips during the HTS test; crack existed at the interface between bond pads and gold bumps. The percentage of gold bumps peeling off of the surface of bond pads increased as HTS test duration increased. Thus, die-shear forces of the chips and flexible substrates assembly were degraded after the HTS test. The reliability of the HTS test for the assembly of chips and flexible substrates with the nickel layer was dominated by crack at the interface between gold bumps and bond pads.

High humidity/high temperature test

Die-shear test after the HH/HT test

The HH/HT test of chips thermosonically bonded onto copper electrodes with the nickel layer showed that die-shear forces had a significant negative correlation with test durations ranging from 0 h to 400 h and then varied within a narrow range as the test durations were further increased from 400 h to 1000 h (Fig.9). Most die-shear forces approached the minimum required by JEDEC standards in specimens subjected to the HH/HT test with test durations from 400 h to 1000 h. All die-shear forces of assemblies of chips and copper electrodes without the nickel layer were far lower than 547gf after the HH/HT test when test durations ranged from 0 h to 1000 h. The low bond strength of chips thermosonically bonded onto flex substrates resulted from weak bonding. Therefore, no further experiments and analyses were required after the HH/HT test for gold bumps thermosonically bonded onto copper electrodes without the nickel layer.

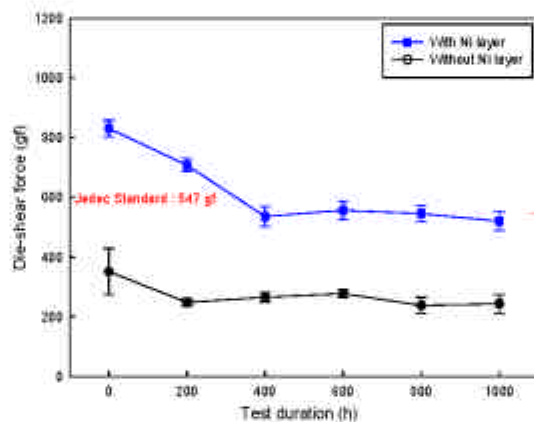


Fig. 9 The die-shear forces of chips thermosonically bonded on flex substrates after subjected to the HH/HT test with various test durations.

Fracture morphology analysis after the HH/HT test

Figure 10 shows the fracture morphology of flex substrates in specimens subjected to 1000-h HH/HT test after the die-shear test. Obviously, the deposited layers on the bond pad were pulled away by the gold bump after the die-shear test, and a round concavity was formed on the bond pad of silicon chips (Fig.10a). Analysis of the fracture morphology showed that this concavity contained a round bond region with a small circumference. To verify possible change in surface morphology of bond pads, this specimen was tilted 30° to examine the fracture morphology using a SEM. The surface morphology of the bond pads showed multiple blisters, some of which were near the bonding region (Fig.10b). Under high magnification, SEM clearly confirmed that the blisters on the bond pad were at bonding region and on the surface of bond pads (Fig.10c and d). During HH/HT test, moisture penetrating the deposited layers of bond pads caused loss of adhesive strength in the deposited layers. Eventually, blisters formed on the bond pad surfaces when the moisture vaporized. The blisters thus deteriorated the die-shear forces in specimens subjected to the HH/HT test. Similarly, a crack occurred at the bond interface between the gold bump and the bond pads in the 200-h HH/HT test (Fig.11a and b). When the test duration of the HH/HT test was increased to 400 h, blisters occurred at the cross section of chips and flex substrates assembly (Figs.11c and d). A slight crack was formed at bond pad of silicon chip after specimen subjected to 200-h HH/HT test, and then the moisture penetrated into the deposited layers of the bond pads as test durations of HH/HT increased. The blister was formed finally due to moisture vaporized in HH/HT test. These observational results can be used to interpret the die-shear forces were significantly deteriorated in specimens subjected to HH/HT test with durations ranging from 0 h to 400 h (Fig. 9).

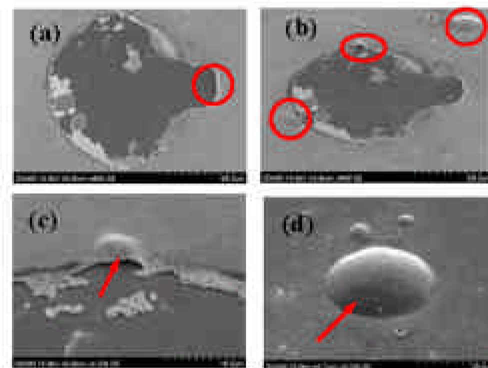


Fig. 10 SEM micrographs of the fracture morphologies of bond pads after die-shear test for specimens subjected to 1000-h HH/HT test, (a) a concavity formed on the surface of bond pads, (b) several blisters was observed on bond pad, (c) a blister occurred at bonding circumference, (d) a large magnification to observe a blister formed on the surface of bond pads.

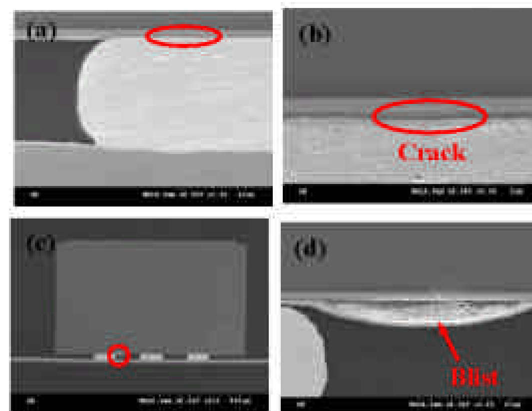


Fig. 11 SEM micrographs show cross section of gold bumps thermosonically bonded onto the flex substrates for specimens subjected to the HH/HT test with various test durations, (a) a gold bump bonded onto copper electrodes after 200-h HH/HT test, (b) a delamination occurred at interface between the gold bump and the bond pad after 200-h HH/HT test, (c) a chip bonded onto flex substrate after 1000-h HH/HT test, (d) a blister occurred at deposited layers of bond pads after 1000-h HH/HT test.

The HH/HT reliability test confirmed good bonding of the gold bumps onto copper electrodes over flex substrates subjected to test duration of 200 h (Fig.11a). However, the crack and blisters that occurred at bond interface between gold bumps and bond pads of silicon chips in HH/HT tests of varying durations deteriorated the die-shear forces. The blisters resulted from moisture penetrating the deposited layers of bond pads before being vaporized. To enhance the reliability of HH/HT test, preventing moistures from penetrating the deposited layers of bond pads is essential.

Conclusions

A 0.5μm-thick nickel layer deposited on copper electrode surfaces effectively enhanced the die-shear forces of chips and the flex substrates assemblies by using a thermosonically bonding. Die-shear forces decreased slightly after the HTS test with various test durations. The percentage of gold bumps peeling off of bond pads on silicon chips increased as HTS test duration increased. Crack was observed at the bond interface between gold bumps and bond pads of chips. This crack was due to thermal stress during the HTS test. However, the FEAES result demonstrates that a sound bond can be achieved between gold bumps and copper electrodes. Thus, the reliability of the HTS test for the chips and flexible substrates assembly was dominated by crack at the interface between gold bumps and bond pads.

The HH/HT test performed at varying durations showed adequate reliability in confirming that gold bumps were firmly bonded onto copper electrodes over flex substrates. However, a crack occurred at the bond interface between the gold bump and the deposited layers of bond pads in specimens subjected to 200-h HH/HT test. As the duration of the HH/HT tests increased, formation of blisters on the surfaces of bond pads increased. Moistures penetrating the deposited layers of bond pads during HH/HT test decreased the adhesive strength of the deposited layers. Eventually, blisters formed when the moistures vaporized. Cracks and blisters degraded the die-shear forces in specimens subjected to HH/HT test at various test durations.

To obtain a good reliability of HTS and HH/HT tests on chips thermosonically bonded directly onto flex substrates, reducing the thermal stress during the HTS test and preventing moisture from penetrating into deposited layers of bond pads during HH/HT test are essential.

Acknowledgments

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四、建議：

1.**此一國際會議，國外專業人士投稿數量或品質均大量提升，今年特別將會議地點改為風光明媚之廣西桂林，吸引更多外籍人士與會，對會議品質具正面提升，故建議國內學辦國際會議時，亦可考慮將會議地點移往風景較佳之地區，除專業的學術會議外，亦可使參與會議學者放鬆平時的工作壓力，對提升外籍人士的參與應有正面的助益。**

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六、活動照片(具代表性之活動照片)：

攝於 2012 **年** 8 **月** 13 **日**, **照片內容簡述：於會議報告會場拍攝照片。**

國科會補助計畫衍生研發成果推廣資料表

日期:2012/11/05

國科會補助計畫	計畫名稱: 以表面活化接合技術開發矽晶片與基板之室溫覆晶接合製程與其接合機理之研究
	計畫主持人: 莊正利
	計畫編號: 100-2221-E-040-008-　　學門領域: 加工與製造
研發成果名稱	(中文) 以表面活化接合技術開發晶片與基板之室溫覆晶接合製程與其接合機理之研究
	(英文) Study on the bonding mechanism and process development for the assembly of chips and substrates at room temperature using surface activated bonding technique
成果歸屬機構	中山醫學大學　發明人(創作人): 莊正利, 楊博智
技術說明	(中文) 試片於於大氣下,金凸塊熱壓覆晶接合於銅電極,以剪力測試量測金凸塊與銅電極之接合強度,並進行橫截面與破斷面之觀察。實驗結果顯示銅電極與金凸塊均經電漿活化之熱壓覆晶接合試片,其剪力值為四者最高,其次為銅電極受氬氣電漿活化處理,但金凸塊未受活化處理之試片,而剪力值最低之試片為金凸塊與銅電極均為受氬氣電漿活化處理。由金凸塊與銅電極之接合介面觀察得知金凸塊與銅電極均經氬氣電漿活化處理者,其接合介面最為完整,無脫層(delamination)或裂縫等缺陷,經氬氣電漿活化處理後之銅電極表面由歐傑電子儀之表面分析結果得知表面之碳含量下降,且接觸角變小,證實氬氣電漿活化處理可有效降低銅電極與金凸塊表面之污染物,進而提高金凸塊與銅電極之熱壓覆晶接合強度。此實驗結果亦驗證電漿活化技術運用於大氣下,熱壓覆晶接合金凸塊與銅電極之可行性。
	(英文) The improvement of the die-shear force was attributed to a better bonding surface of gold bumps and copper electrodes obtained owing to the containments on the surface of the bonding materials was removed by the argon plasma. For gold bumps and copper electrodes were activated by argon plasma, neither delamination nor crack is found at bonding interface between gold bumps and copper electrodes. A low contact angle was also determined on the surface of copper electrodes after argon plasma activated, indicating a clean bonding surface was achieved. A clear atomic interdiffusion between gold bumps and copper electrodes was observed for specimens were subjected to argon plasma activation. The argon plasma activation was an effective scheme to improve the bonding strength of the assembly of chips and substrates. Thus, the argon plasma activation has great potential to be applied to chips and substrates assembly using thermal compression bonding process.
產業別	電機及電子機械器材業
技術/產品應用範圍	微電子構裝技術/微電子
技術移轉可行性及預期效益	提高金凸塊與銅電極之接合品質

註:本項研發成果若尚未申請專利,請勿揭露可申請專利之主要內容。

100 年度專題研究計畫研究成果彙整表

計畫主持人：莊正利	計畫編號：100-2221-E-040-008-
計畫名稱：以表面活化接合技術開發矽晶片與基板之室溫覆晶接合製程與其接合機理之研究	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	1	1	100%		29 屆中華民國機械工程師年會，高雄。
		專書	1	1	100%		楊博智，中正大學機械研究所碩士論文(2012 年 7 月)。
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	1	1	100%	人次	楊博智
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	1	100%	篇	投稿論文改寫中。
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：（以 100 字為限）

本研究計畫目前已發表於 29 屆機械年會之口頭報告文，目前正將實驗結果改寫為國際學術期刊之投稿論文，預計年底前投稿至 Surface & coating Technology 期刊。

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

1.本研究成功以氬氣電漿清除金凸塊與銅電極表面之污染物，並使其平均剪力值高於高於業界之要求，而由 Auger 電子儀之分析結果得知金凸塊與銅電極之主要污染物為碳與氧化膜，而經氬氣電漿活化之金凸塊或銅電極其表面之碳含量均大幅下降，可有效促進金凸塊與銅電極之接合，進而提高其接合品質，此一接合機理已於本計畫中完整驗證，預期可將該結果發表於國際學術期刊。但銅電極表面之銅電極仍殘留部分氧化物，顯示物理性之氬氣電漿不適合去除氧化膜，故由此實驗結果得知當電漿活化處理時，加入少量之氫氣還原性電漿，應可去除銅電極表面之氧化膜，此部分延伸性研究目前正持續進行中。

2.本研究結果除可提供封裝業界選用活化電漿之參考資料外，更顯示金凸塊與銅電極於室溫環境接合之可行性，可提高業界開發室溫接合先進技術之基礎。