科技部補助專題研究計畫成果報告
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以表面活化技術提高非導電膠接合矽晶片與軟性基板之接合強度與可靠度

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中 文 摘 要 ： 本研究結合熱壓接合製程與非導電膠(non-conductive paste, NCP)將晶片覆晶接合於軟性基板，藉由軟性基板與晶片凸塊表面進行物理性之氬氣電漿活化處理，期望提升晶片與軟性基板之接合強度。經氬氣電漿活化後試片以非導電膠與熱壓接合製程進行接合，量測軟性基板經表面活化處理後之接觸角，評估其潤濕性；以化學光譜儀(ESCA)分析軟性基板表面經電漿活化處理後之組成元素；以原子力顯微鏡(AFM)量測試片之表面粗糙度，用以驗證表面活化處理之效用；接合後之試片以剪力測試檢測晶片與軟性基板之接合強度；以電子顯微鏡(SEM)與能量分析儀(EDS)觀察剪力測試之破斷面與其相關之組成元素，用以判斷晶片與軟性基板於剪力試驗時之破斷模式。實驗結果顯示經活化處理後之晶片以非導電膠與熱壓製程可成功接合於軟性基板，並由接合試片之橫截面顯微結構得知金凸塊與軟板間之接合界面完整，未發現脫層或空孔等缺陷，且金凸塊與軟板表面之接著界面未殘留非導電膠，晶片與軟板間形成良好之電訊通路；由剪力試驗結果得知經氬氣電漿活化處理後，晶片與軟板接合試片之剪力值均高於未進行表面活化處理者，且由剪力試驗後之破斷面分析得知未經表面活化處理之接合試片，其破裂模式為晶片與非導電膠從軟性基板表面剝離(peel-off)，此為非導電膠與軟板之接著性不佳所致；反觀經氬氣電漿活化處理之接合試片，其斷裂發生於固化之非導電膠處，晶片與軟板表面均殘留固化之非導電膠，顯示非導電膠與軟性基板之接合強度高於固化之非導電膠強度。此一實驗結果說明氬氣電漿表面活化處理有助於提升晶片與軟性基板之接合強度，進一步分析經表面活化處理軟板表面之組成與潤濕性，可清楚發現軟板表面之汙染物降低且接觸角大幅降低，驗證氬氣電漿活化處理確實可移除軟板表面之汙染物，提高非導電膠與軟性基板之潤濕性，進而提升晶片以非導電膠接著於軟性基板之接合強度，經氬氣電漿處理後之軟性基板放置於防潮箱不同時間後，發現晶片與軟性基板之接合強度隨儲存時間增加而下降，顯示經氬氣電漿處理軟性基板表面易受污染而降低其表面之潔淨度，進而判斷晶片與軟性基板之接合強度，特將經氬氣電漿處理後之軟板，放置於防潮箱中經過不同儲存時間後，再與晶片進行接合，並以剪力試驗測試晶片與軟板之接合強度，用以評估氬氣電漿之效果。

中文關鍵詞： 非導電膠、覆晶接合、電漿活化技術

英 文 摘 要 ： Argon plasma was selected to perform the surface activation on the surface of flex substrates in this study. This argon plasma activation technology was

expected to remove the surface contaminants, and to reduce the bonding barrier between flex substrates and the NCP. The bonding strength of chips and flex substrates assembly is thus improved. With Appropriate bonding parameters, a solid bonding interface can be obtained for chips and flex substrates assembling with NCP and thermal compression bonding process. Neither porosity nor delamination was found at bonding interface between gold bumps and copper electrodes of flex substrates. The NCP was removed from the surface of flex substrates during thermal bonding process, and gold bumps bonded on copper electrodes directly. An electrical path between chips and the flex substrates was formed. In contrast to flex substrates without argon plasma activating, the die-shear force was significant enhancement for chips and flex substrates were activated with argon plasma. A low contact angle can be determined on the surface of flex substrates, indicating the containments can be removed by argon plasma, and then a clean bonding surface was achieved for flex substrates activating with argon plasma. After die-shear test, the fracture mode of NCP was peeling off from the surface of flex substrates for flex substrates without activating with argon plasma, indicating the bonding strength of NCP and flex substrates is poor. For flex substrates subjected argon plasma activation, the residual NCP can be found on the both sides of flex substrate and chip, indicating the bonding strength of NCP and flex substrates is even higher than the strength of NCP itself. These experimental results can be used to interpret that argon plasma activation was an effective scheme to improve the bonding strength of chips and substrates assembling with NCP and thermal compressing bonding process. As extending storage durations for flex substrates activated with argon plasma, the bonding strength of chips and flex substrates assembly degraded significantly, implying the property of bonding surface was deteriorated when the specimen were exposed in an air atmosphere. According with our experimental result, the storage

duration should be below one day for flex substrates activated with argon plasma.

英文關鍵詞： Non-conductive paste, flip-chip bonding, plasma activated technology

目錄

中文摘要

本研究結合熱壓接合製程與非導電膠(non-conductive paste, NCP)將晶片覆晶接合於軟性基板，藉由軟性基板與晶片凸塊表面進行物理性之氬氣電漿活化處理，期望提升晶片與軟性基板之接合強度。經氬氣電漿活化後試片以非導電膠與熱壓接合製程進行接合，量測軟性基板經表面活化處理後之接觸角，評估其潤濕性；以化學光譜儀(ESCA)分析軟性基板表面經電漿活化處理後之組成元素；以原子力顯微鏡(AFM)量測試片之表面粗糙度，用以驗證表面活化處理之效用；接合後之試片以剪力測試檢測晶片與軟性基板之接合強度；以電子顯微鏡(SEM)與能量分析儀(EDS)觀察剪力測試之破斷面與其相關之組成元素，用以判斷晶片與軟性基板於剪力試驗時之破斷模式。實驗結果顯示經活化處理後之晶片以非導電膠與熱壓製程可成功接合於軟性基板，並由接合試片之橫截面顯微結構得知金凸塊與軟板間之接合界面完整，未發現脫層或空孔等缺陷，且金凸塊與軟板表面之接著界面未殘留非導電膠，晶片與軟板間形成良好之電訊通路；由剪力試驗結果得知經氬氣電漿活化處理後，晶片與軟板接合試片之剪力值均高於未進行表面活化處理者，且由剪力試驗後之破斷面分析得知未經表面活化處理之接合試片，其破裂模式為晶片與非導電膠從軟性基板表面剝離(peel-off)，此為非導電膠與軟板之接著性不佳所致；反觀經氬氣電漿活化處理之接合試片，其斷裂發生於固化之非導電膠處，晶片與軟板表面均殘留固化之非導電膠，顯示非導電膠與軟性基板之接合強度高於固化之非導電膠強度。此一實驗結果說明氬氣電漿表面活化處理有助於提升晶片與軟性基板之接合強度，進一步分析經表面活化處理軟板表面之組成與潤濕性，可清楚發現軟板表面之汙染物降低且接觸角大幅降低，驗證氬氣電漿活化處理確實可移除軟板表面之汙染物，提高非導電膠與軟性基板之潤濕性，進而提升晶片以非導電膠接著於軟性基板之接合強度，經氬氣電漿處理後之軟性基板放置於防潮箱不同時間後，發現晶片與軟性基板之接合強度隨儲存時間增加而下降，顯示經氬氣電漿處理軟性基板表面易受污染而降低其表面之潔淨度，進而判斷晶片與軟性基板之接合強度，特將經氬氣電漿處理後之軟板，放置於防潮箱中經過不同儲存時間後，再與晶片進行接合，並以剪力試驗測試晶片與軟板之接合強度，用以評估氬氣電漿之效果。

*關鍵字：*非導電膠、覆晶接合、電漿活化技術

Abstract

Argon plasma was selected to perform the surface activation on the surface of flex substrates in this study. This argon plasma activation technology was expected to remove the surface contaminants, and to reduce the bonding barrier between flex substrates and the NCP. The bonding strength of chips and flex substrates assembly is thus improved. After flex substrates were activated with argon plasma, several analytical methods were applied to verify the effective of argon plasma activated technology on the bonding surface of flex substrates, such as the contact angle was measured to verify the wettability of flex substrates, the ESCA was employed to determine the compositions on the surface of flex substrates, the AFM was conducted to examine the changes of roughness on the bonding surface of flex substrates, and die-shear test was used to evaluate the bonding force of chips and flex substrates assembly. With Appropriate bonding parameters, a solid bonding interface can be obtained for chips and flex substrates assembling with NCP and thermal compression bonding process. Neither porosity nor delamination was found at bonding interface between gold bumps and copper electrodes of flex substrates. The NCP was removed from the surface of flex substrates during thermal bonding process, and gold bumps bonded on copper electrodes directly. An electrical path between chips and the flex substrates was formed. In contrast to flex substrates without argon plasma activating, the die-shear force was significant enhancement for chips and flex substrates were activated with argon plasma. A low contact angle can be determined on the surface of flex substrates, indicating the containments can be removed by argon plasma, and then a clean bonding surface was achieved for flex substrates activating with argon plasma. After die-shear test, the fracture mode of NCP was peeling off from the surface of flex substrates for flex substrates without activating with argon plasma, indicating the bonding strength of NCP and flex substrates is poor. For flex substrates subjected argon plasma activation, the residual NCP can be found on the both sides of flex substrate and chip, indicating the bonding strength of NCP and flex substrates is even higher than the strength of NCP itself. These experimental results can be used to interpret that argon plasma activation was an effective scheme to improve the bonding strength of chips and substrates assembling with NCP and thermal compressing bonding process. As extending storage durations for flex substrates activated with argon plasma, the bonding strength of chips and flex substrates assembly degraded significantly, implying the property of bonding surface was deteriorated when the specimen were exposed in an air atmosphere. According with our experimental result, the storage duration should be below one day for flex substrates activated with argon plasma.

Keywords: **Non-conductive paste, Flip-chip bonding, Plasma activated technology**

1.前言

晶片與硬式基板(rigid substrate)之覆晶接合製程依其接合能量，可分為熱壓接合(thermal compressive bonding, TCB) [1]、超音波接合(ultrasonic bonding) [2]與熱音波接合(thermosonic bonding, TSB) [3]。熱壓接合之主要關鍵參數為接合負荷(bonding load)與載台溫度(stage temperature)，接合負荷主要使晶片凸塊與基板電極緊密接觸，藉由載台之加熱溫度使接合界面原子相互擴散而鍵結，然而矽晶片屬脆性材料，無法承受過大之接合負荷，因此為提高晶片與基板之接合強度，需大幅提高載台之加熱溫度，但軟性基板之玻璃轉換溫度(Tg)與剛性(rigidity)較硬式基板為低，故軟性基板無法承受較高之加熱溫度且高溫下易使軟性基板變形而難以定位接合，此一接合技術不適用於晶片與軟性基板之覆晶接合；超音波接合技術係於接合過程中，以超音波功率(ultrasonic power)使接合材料相互摩擦，該摩擦熱可提升接合界面溫度，進而軟化接合界面材料，造成塑性變形(plastic deformation)而接合，故超音波覆晶接合之關鍵參數為輸入之超音波功率，從過去研究結果顯示過大之超音波功率，易造成晶片(特別是化合物晶片)產生彈坑孔(crater)缺陷 [4]，進而使凸塊由晶片上脫離，造成封裝電訊通路之失效(failure)。此外，軟性基板之剛性較硬式基板為低，部分超音波功率易為軟性基板所吸收，無法將超音波有效傳遞至晶片與軟性基板之接合界面，故此一技術亦不適用於晶片與軟性基板之接合。

熱音波覆晶接合技術則結合前兩項技術之優點，其主要之關鍵參數為接合負荷、載台加熱溫度與超音波功率，晶片與硬式基板進行熱音波覆晶接合時，載台加熱溫度提供接合界面原子交互擴散所需熱能，並供給超音波能量，超音波功率除提高接合界面之溫度 [5]，有助接合界面原子交互擴散外，超音波能量更可使接合界面之材料瞬時間累積大量差排，促使接觸金屬面產生動態應變軟化(dynamic strain softening)，有助於接合界面材料之接合，適量超音波能量可降低矽晶片與硬式基板之接合溫度，進而提高其製程之可靠度。若將熱音波接合技術應用於矽晶片與軟性基板之覆晶接合，因軟性基板之剛性(rigidity)不足，軟性基板易吸收部分超音波功率，難以將其能量傳遞至晶片與軟性基板之接合界面，且軟性基板之玻璃轉換溫度較硬式基板為低，故無法於加熱載台進行較為高溫之加熱，過高之加熱溫度可能造成軟性基板之軟化變形或難以夾持 [6]，顯然此技術若應用於晶片與軟性基板之覆晶接合仍須克服上述之挑戰。

綜整上述晶片與硬式基板覆晶接合製程之特性，該製程若應用於晶片與軟性基板之接合，必遭遇軟性基板機械性質不佳之多項挑戰，為提供晶片與軟性基板覆晶接合之技術需求，覆晶膠合(flip-chip with adhesive)製程便因應而生，此一製程為目前封裝業界進行晶片與軟性基板接合之主要技術，該技術係於軟性基板上塗佈膠合物質後，再以傳統之熱壓覆晶製程將晶片反轉貼合於塗佈膠合物質之軟性基板上，待其膠合物質固化(cured)後，即完成晶片與軟性基板之接合。晶片與軟性基板覆晶膠合之強度主要來自膠合物質之固化強度(cured strength) [7]，故無須提供過高之接合負荷與載台加熱溫度，上述晶片與軟性基板覆晶接合之挑戰即可迎刃而解。目前業界廣泛應用於晶片與軟性基板覆晶接合之膠合物質為異方性導電膠(anisotropic conductive paste, ACP)，該膠合材料係於熱固型(thermal setting type)之高分子樹脂(polymer resin)中填入導電顆粒，藉由導電顆粒於樹脂中之接觸而形成電訊通路，填充於樹脂中之導電顆粒數目對晶片與軟性基板封裝後之電性具關鍵性影響，若填充導電顆粒過多，易於晶片凸塊間形成架橋而短路 [8]；

填充量不足，導電顆粒無法達成電訊通路連接之封裝目的，顯然異方性導電膠仍存在難以控制之製程參數。故覆晶膠合製程之研究已由過去之異方性導電膠轉移至非導電膠(non-conductive past, NCP) [9]，非導電膠之接合方式係於晶片凸塊與軟性基板電極間，塗佈一層非導電膠，當非導電膠固化後縮收，使晶片凸塊與軟性基板電極接觸而維持導電通路，因非導膠無須填充導電顆粒，可免除填充導電顆粒數量之相關問題，且填充之導電顆粒為銀等高導電性材料 [10]，其價格昂貴，故非導電膠之價格較異方性導電膠為低，導入非導電膠於晶片與軟性基板之封裝接合製程，應可有效降低生產成本。

顯然晶片與硬式基板之傳統覆晶接合製程已無法滿足晶片與軟性基板接合之技術需求，開發新式之封裝接合製程以符合晶片與軟性基板接合之技術需求，實為必行趨勢。本計畫申請人過去曾在國科會經費補助下，探討非導電膠結合熱音波覆晶製程對 RFID 晶片與軟性基板接合之可行性與可靠度之研究，該研究結果顯示 [11-12]熱音波覆晶製程之超音波功率可有效移除軟性基板銅電極上之非導電膠，使晶片之金凸塊成功與軟性基板之銅電極接著，形成良好之電訊通路，但晶片與軟性基板之接合強度偏低 [11]，且隨後進行高壓蒸煮(pressure cooker test, PCT)之可靠度試驗結果顯示非導電膠與軟性基板表面之接合性不佳，接合界面產生剝離之破壞模式，水氣由接合界面剝離處滲入晶片與軟性基板之接合區域，隨後晶片與軟性基板完全分離，其可靠度無法滿足業界之要求 [12]，相似之實驗結果亦出現國內封裝廠之研究報告中 [13-14]。非導電膠之主要技術瓶頸為非導電膠與軟性基板之接合性不佳，進而影響後續之可靠度測試結果，若能改善非導電膠與軟性基板之接合品質，必能大幅提昇該技術於實際生產之應用性。

泛用之電漿氣體可分為物理性活化(physical activated) [15]與反應性活化(reactive activated) [16]兩大機制，前述物理性活化係以惰性氣體在低壓(low pressure)狀態下，以高頻電壓(high frequency voltage)激發為離子狀態，該離子以高速運動撞擊材料表面，移除材料表面之氧化膜(oxide layer)或污染物(contaminant)，達到活化材料表面之功能；反應性活化通常應用於材料表面有機物之活化，電漿氣體選用氧氣、氫氣或兩者與惰性氣體之混合氣體，氧離子可與碳-氫有機物反應形成二氧化碳與水，而該反應物可用抽氣系統排至大氣環境，其化學反應式為：$CxHyOz+(O^*_2,O)\rightarrow CO_2+H_2O$ [16]。選擇電漿活化氣體對材料表面污染物之清潔效果影響甚鉅，故應依材料之特性與污染物之種類選擇適當之電漿活化氣體。Gene Dunn [17]將電漿表面活化技術應用於晶片金凸塊與基板金電極之接合，選用氬氣電漿進行基板金電極之表面活化處理，隨後金凸塊以熱音波覆晶接合於基板金電極，並以剪力測試其接合強度，實驗結果顯示經氬氣電漿活化處理之試片，其破斷模式為金凸塊殘留於基板電極，且金凸塊殘留於基板金電極之百分比增加，金凸塊與基板金電極之接合強度亦隨之提高，並配合歐傑電子儀表面元素之分析結果，證實氬氣電漿可移除基板金電極表面之污染物，降低接合能障(bonding barrier)，進而提高其接合強度。

相對於傳統覆晶結合製程，結合非導電膠與熱壓覆晶製程應用於晶片與軟性基板之接合具有許多優勢，但非導電膠與軟性基板之接合品質不佳，且晶片與軟性基板接合後試片無法通過相關之可靠度試驗，致使該製程目前仍無法運用於量產，若將電漿表面活化技術導入非導電膠與熱壓覆晶製程中，藉由電漿表面活化技術降低軟性基板表面之接合能障，必可提高非導電膠與軟性基板之接合強度，有助於提高該製程之實際應用性。

2.研究目的

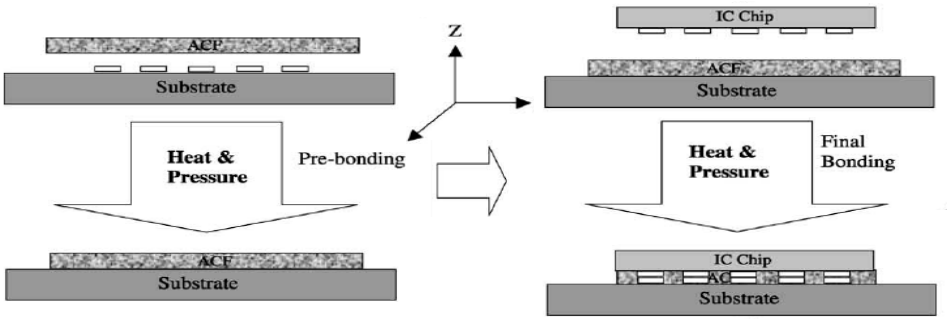
近年來消費性電子產品蓬勃發展，特別是各項可攜帶之通訊產品，而攜帶式消費性電子講求輕、薄、短、小與易於攜帶之方便性，因此軟性基板(flex substrate)已取代原有硬式基板而廣泛被使用，然而軟性基板之剛性(rigidity)較硬式基板為低，當晶片與軟性基板進行熱音波覆晶接合時，軟性基板易吸收部分超音波功率能量，難以使晶片凸塊與軟性基板電極形成良好之接合，故目前晶片與軟性基板之接合大部分採用覆晶膠合(flip-chip bonding with adhesive)。目前業界主要以異方性導電膠(anisotropic conductive paste, ACP)接合晶片與軟性基板，但異方性導電膠添加導電顆粒之數量對其接合品質產生嚴重挑戰，若添加導電顆粒太多，易產生聚集而發生電訊通路短路，反之導電顆粒添加數量太少，晶片凸塊無法與軟性基板電極形成良好電訊通路，故無須添加導電顆粒之非導電膠便成為先進封裝技術之研究主流 [13-14]。本計畫申請人曾進行非導電膠之熱音波覆晶接合製程與其可靠度之研究 [11-12]，結果顯示熱音波覆晶製程之超音波功率有效清除軟性基板電極上之非導電膠，使晶片凸塊與軟性基板電極接觸而形成良好之電訊通路，但其接合強度偏低且接合後試片之可靠度不佳，主要原因為接合強度主要來自非導膠固化時與軟性基板之接合強度，軟性基板表面可能存在加工製程所殘存之污染物，故非導電膠無法與軟性基板形成良好之接著，然而非導電膠若無法與軟性基板形成良好之接著，於高壓蒸煮(pressure cooker test)可靠度測試時，高壓水氣由接合界面之缺陷處滲入，進而造成晶片與軟性基板之分離，故無法維持良好之可靠度。

本研究主要探討電漿表面活化軟性基板對晶片與軟性基板以非導電膠熱壓覆晶接合強度之影響，藉由電漿表面活化實驗參數之改變，建立適合軟性基板之電漿活化參數，如電漿氣源種類、功率、活化時間、艙體真空度等，並觀察軟性基板表面經電漿活化處理後之表面型態(surface morphology)與組成(composition)之改變，隨後將非導電膠塗佈於軟性基板上，進行晶片與軟性基板之熱音波覆晶接合實驗，待晶片與軟性基板接合後，以剪力試驗(die-shear test)量測軟性基板與晶片之接合強度，以電子顯微鏡(SEM)觀察非導電膠與軟性基板之接合界面是否完整，並判斷接合試片經剪力試驗後之破斷模式(fracture mode)，藉以建立電漿表面活化技術提升非導電膠接合晶片與軟性基板強度之機理。

3.文獻探討

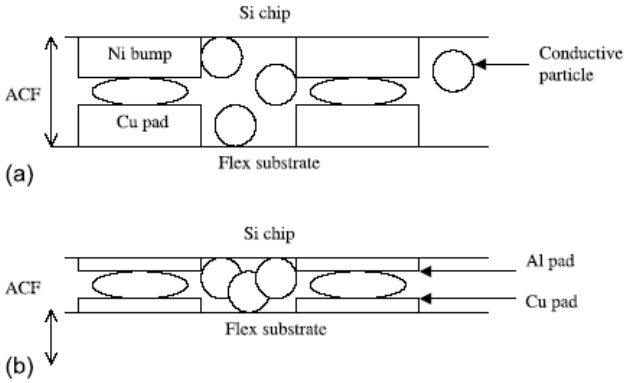
3.1覆晶膠合製程

軟性基板之剛性與玻璃轉化溫度均遠低於硬式基板，晶片與軟性基板難以沿用傳統覆晶製程進行接合，目前封裝業界多以異方性導電膠接合製程進行晶片與軟性基板之接合，主要應用產品為顯示器驅動晶片(displays driver IC)與可攜帶式電訊產品之封裝，圖一為異方性導電膜封裝製程之示意圖 [18]，以加壓、加熱方式將該異方性導電膜預接合(pre-bonding)於軟性基板上，隨後晶片以熱壓覆晶製程將晶片凸塊反轉接合於軟性基板電極，完成晶片凸塊與軟性基板電極之電訊通路連接。



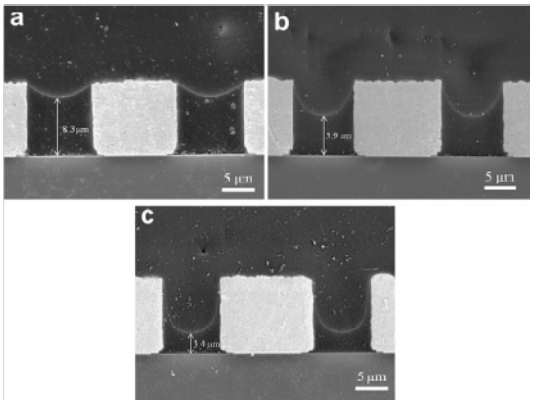
圖一：異方性導電膠模應用於晶片與軟性基板之覆晶接合 [18]

異方性導電膠內填充導電顆粒之目的為提供晶片凸塊與軟性基板電極於垂直方向(z 方向)之電訊通路連接，導電顆粒在晶片凸塊與軟性基板電極間相互接觸而形成電訊通路，故導電顆粒之數量與其分散之均勻性，對晶片與軟性基板之電訊通路品質極為關鍵，晶片凸塊間之水平方向(x-y 平面)需為絕緣，以避免軟性基板電極因導電顆粒架橋(bridge)而產生電訊通路之短路(short circuit)。異方性導電膠之封裝技術隨晶片間距降低，導電顆粒之平均直徑亦從 10 μm、5 μm 降至 3μm，就目前技術之發展趨勢，平均直徑 3 μm 之導電顆粒應為技術極限，當導電顆粒尺寸細化，粒子間易團聚(cluster)而難於高分子樹脂中均勻分散 [19]。此外，當導電顆粒直徑細化，為確保垂直方向電訊通路之導通，須提高導電顆粒之添加量，但也可能造成水平方向導電顆粒聚集，造成短路，如圖二所示 [19]，故對細間距、高接點數之驅動晶片而言，異方性導電膠之接合製程，仍存在高度風險與不確定性。

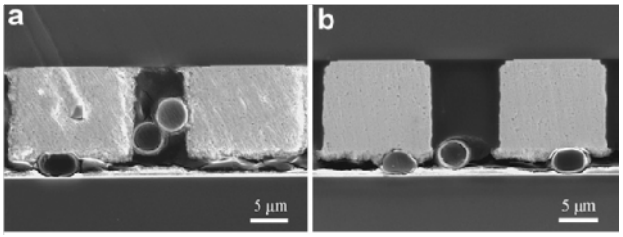


圖二：晶片凸塊與軟性基板電極以異方性導電膠接合示意圖，(a)導電顆粒均勻分散之接合，(b)導電顆粒團聚形成短路 [19]。

為滿足異方性導電膠及細間距、高接點數之驅動晶片封裝製程，Hong 等人[20]以感光絕緣膠旋塗於測試晶片金凸塊，藉由光暴露時間使凸塊側壁形成一絕緣層，且控制絕緣膠黏度分別以未稀釋(100 %)、50 %、66.7 %製作絕緣層外形，如圖三所示 [20]，可觀察到該絕緣層完整塗覆於凸塊側緣，能有效阻絕異方性導電膠之導電顆粒於相鄰凸塊間接觸形成電氣短路，亦集中導電顆粒於焊墊及凸塊間，增加試片之電訊通路傳導，另外防止晶片金凸塊於接合過程中變形而影響試片接合品質，如圖四所示 [20]，此結果說明成功以異方性導電膠結合玻璃覆晶製程，製造出細間距晶片金凸塊與基板之接合試片，有效降低封裝元件尺寸及晶片與基板接合試片電阻率，但此製程須精準控制絕緣膠含量、黏度與外形，必大幅增加生產成本，且用於接著晶片與基板之異方性導電膠膠量減少，有影響試片接合強度之疑慮，因此實際應用在半導體產業仍有待商榷。

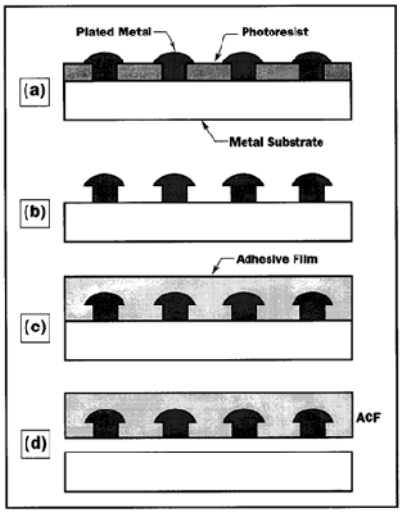


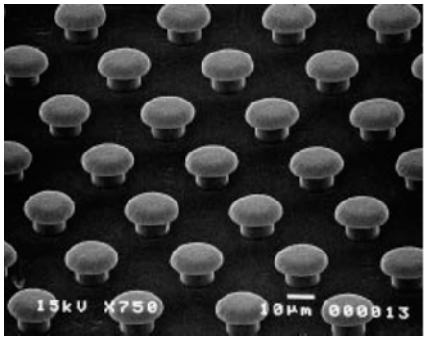
圖三：晶片凸塊之絕緣層橫截面圖，(a)未稀釋(100%)，(b)66.7%，(c)50%之黏度 [20]。



圖四：晶片凸塊與基板接合試片之橫截面接合界面，(a)未塗覆絕緣層，(b) 凸塊側緣塗覆未稀釋(100%)之絕緣層 [20]。

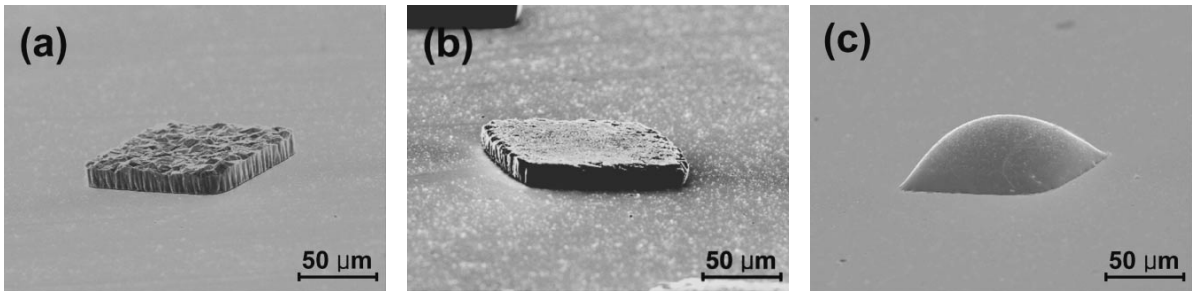
Plam 等人 [21]添加含量不等之導電顆粒於異方性導電膠中，用以接合晶片金凸塊與軟性基板電極，並探討導電顆粒含量對金凸塊與電極間電訊通路之影響，實驗結果指出凸塊與電極接合後，電訊通路之電阻隨導電顆粒增加而降低；而採用不同的導電顆粒時，凸塊與電極界面之接合型態亦有所不同，當導電顆粒表面為鎳與金鍍層時，在相同接合條件下，導電顆粒之變形量最大；若導電顆粒為不規則形狀之鎳顆粒或圓形鎳顆粒時，因鎳顆粒硬度較高分子樹脂為高，故鎳顆粒可有效穿越高分子膠，刮除凸塊上之氧化物，凸塊與電極之電訊通路品質得以提升，若異方性導電膠之導電顆粒無法均勻分佈於高分子樹脂中，進行覆晶接合製程時，凸塊與電極間，可能因缺乏導電顆粒而無法形成電訊通路。Ishibash 等人 [22]以半導體泛用之曝光、顯影、金屬沈積與蝕刻等標準製程，將高度為 12μm、直徑約 20μm 之鎳柱均勻鍍著於異方性導電膜上，使其成為面積陣列鎳柱，如圖五所示 [22]，該製程可確保垂直方向之電訊導通，且水平方向為電訊之絕緣，含鎳柱之異方性導電膜於熱壓過程，使鎳柱與凸塊、電極形成良好之電訊通路，此一製程雖可確保鎳柱於晶片凸塊與基板電極間形成良好之電訊通路，且不致因導電顆粒團聚而發生架橋短路之缺陷，但此異方性導電膠之製作需引入半導體之相關製程，必大幅提升異方性導電膠之生產成本，故此一製程之實際應用性備受挑戰。非導電膠無須填充導電顆粒且生產成本遠低於異方性導電膠，故以非導電膠接合晶片與軟性基板，為高階軟板封裝製程之發展趨勢。





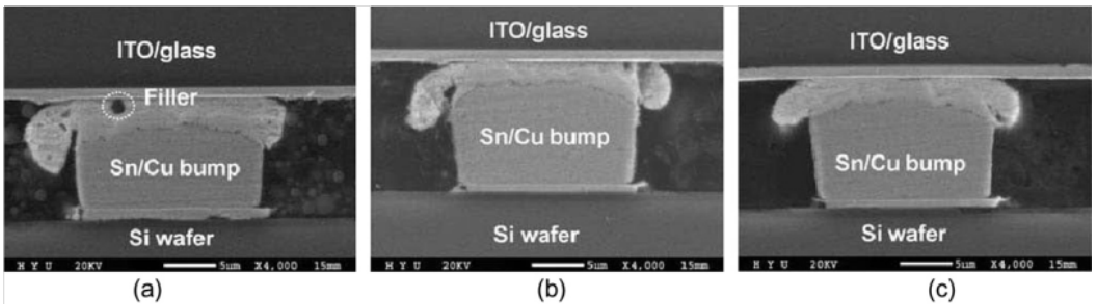
圖五：以半導體標準製程將鎳柱沈積於異方性導電膠上，使其成為面積陣列之鎳柱 [22]。

非導電膠主要為熱固型高分子樹脂與不等比例之絕緣填充物(filler)所組成[23]，因此非導電膠之固化溫度與固化時間對非導電膠之品質具關鍵性影響，固化溫度太低或固化時間不足，易造成非導電膠固化不全，無法提供晶片與基板良好之接合強度，反之若固化溫度過高，非導電膠產生快速固化，空孔或氣泡等缺陷殘留於固化之非導電膠中，對非導電膠之接合強度產生不良影響。Chiang 等人 [24]指出固化參數不佳易造成非導電膠內存在空孔或氣泡，其原因為水氣吸附於晶片或基板表面，非導電膠快速固化過程時，水氣無法及時離開非導電膠，因而殘存於非導電膠中，改善建議為封裝前先行低溫烘烤晶片或軟板以去除表面之水氣；Lee 等人 [25]以非導電膠接合晶片與基板，設計三種不同處理狀態之錫凸塊與電極接合，分別為電鍍之錫凸塊(as electroplated Sn bump)、電鍍後經熱壓整平之錫凸塊(coined Sn bump)與電鍍後經迴銲錫凸塊(reflowed Sn bump)，如圖六所示 [25]。相同熱壓覆晶膠合製程參數下，經迴銲錫凸塊與基板電極之接觸電阻(contact resistance)最低，且由剪力試驗後之破斷面觀察，得知迴銲錫凸塊表面殘留之非導膠最少，顯示經迴銲錫凸塊與電極之接合狀況最佳，因迴銲後錫凸塊表面凸起，該凸起部分於接合時將塗佈於電極上方之非導電膠擠出(squeeze)錫凸塊與電極之接合區域，錫凸塊可與電極直接接著，故兩者間之接觸電阻較低；反觀錫凸塊經整平後之表面平坦，於覆晶膠合時，整平之錫凸塊無法將塗佈於電極之非導電膠擠出，大部分非導電膠殘留於錫凸塊與電極之接合界面，故其電阻較高。綜整上述文獻之研究結果得知，採用非導電膠之覆晶製程接合晶片與基板時，非導電膠之固化參數與晶片凸塊外形對覆晶接合後之品質與接合界面之完整性極為關鍵。



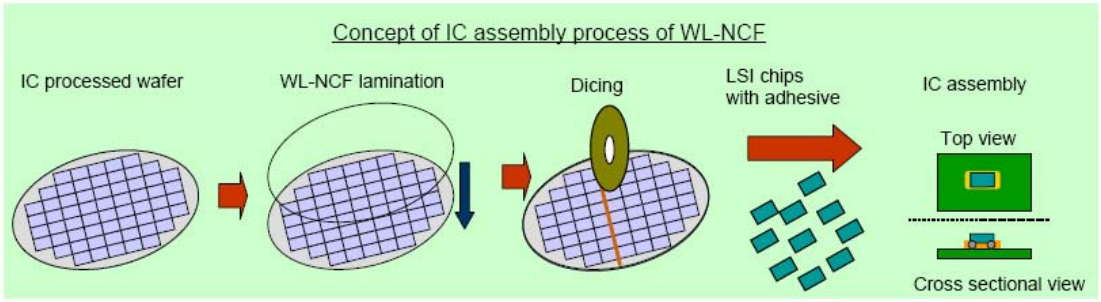
圖六：以電鍍法沈積錫凸塊經不同處理後之外觀圖，(a)經電鍍後，(b)經熱壓整平，(b)經回銲處理 [25]。

Kim 等人 [26]將細間距晶片之 Sn/Cu 凸塊進行迴焊後，以非導電膠熱壓覆晶膠合於玻璃基板，並且比較三種不同絕緣填充物類型之非導電膠對晶片凸塊與基板間接合界面之影響，其絕緣填充物類型分為 NCA-A (filler：silica)、NCA-B (filler：fluoropolymer)及 NCA-C (no filler)，實驗結果顯示以 NCA-A、NCA-B 接合之試片，其接合界面有少許絕緣填充物存在，而 NCA-C 之試片接合界面則接著完整，無孔洞、裂痕等缺陷，如圖七所示 [26]，此結果說明選擇適當種類非導電膠之重要性，但整體而言，以非導電膠熱壓覆晶膠合之接合試片具備良好之接合強度與可靠度。



圖七：以不同種類非導電膠接合晶片凸塊與基板之接合試片橫截面接合界面，(a)NCA-A，(b)NCA-B，(b)NCA-C [26]。

Lee 等人 [27]以非導電膠進行多晶片封裝技術之研究，並與其他接合製程之試片比較差異性，實驗結果發現以非導電膠進行接合之試片，其接合界面未發現裂痕等缺陷，且晶片與基板間之電阻較小，晶片與基板間可形成良好之電訊通路。Nonaka 等人 [28]將非導電膠之覆晶接合製程進一步擴展至晶圓層級封裝(wafer level packaging)，先將非導膠製作成片狀之膠膜(film)，並將該非導電膠膜貼合於晶圓上，隨後進行晶圓之切割，每一晶片表面具貼合之非導電膠，最後將晶片壓接於基板電極即完成封裝，如圖八所示 [28]。此一製程之優勢係將非導電膠膜預貼合於晶圓表面，隨後進行晶圓之切割，可有效降低單一晶片塗佈非導電膠之製程時間。



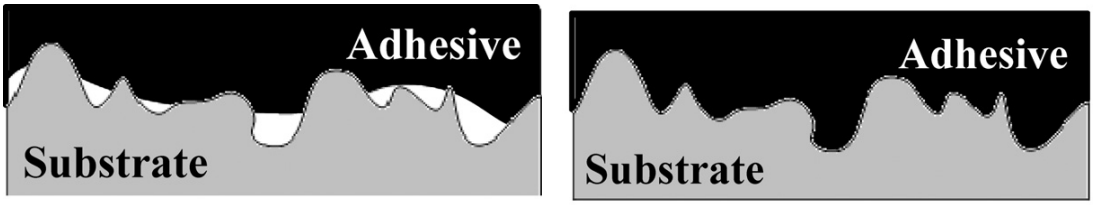
圖八：將非導電膠應用於晶圓層級封裝之示意圖 [28]。

就目前學術期刊或相關學術會議中，大部分均探討異方性導電膠應用於各種晶片與軟性基板之接合，對非導電膠之應用與學理之探討非常有限，但仍可見各大封裝廠進行研究之蹤跡 [13-14]，顯示此一封裝技術深具發展潛力。

3.2 電漿活化技術之應用

電漿表面活化技術係利用氣體電漿活化接合材料之表面，有效去除或降低接合材料表面污染物所形成之能障(barrier)或改變接合材料表面之性質 [29]，進而提高後續材料接合之品質。Ting 等人 [30]使用氫氣/氧氣混合電漿處理鋼板表面以增加鋼板間之接著性，結果顯示材料表面性質與型態受氫氣/氧氣之混合電漿影響而改變，表面接觸角隨電漿功率及活化時間增加而降低，但當電漿活化時間過長時，表面接觸角反而隨之上升，表明電漿活化處理技術能有效使材料潤濕性增加，且須選擇適當電漿活化處理參數。Barshilia 等人 [31]以氬氣/氫氣之混合氣體電漿提升物理鍍膜(PVD)與鋼板之接著性，實驗結果為有效去除鋼材表面之氧化層與污染物，獲得潔淨之鋼材表面外，透過電漿活化技術對鋼板表面產生之粗糙度亦可提升鍍膜與鋼板之黏著性。Lee 等人 [32]以氬氣與氧氣電漿進行鋼材表面之活化處理，實驗結果顯示經氬氣電漿表面活化處理後，鋼材與黏膠之剪切強度可提高 23%，因氬氣電漿可有效移除鋼材表面之污染物，提高鋼材與膠合

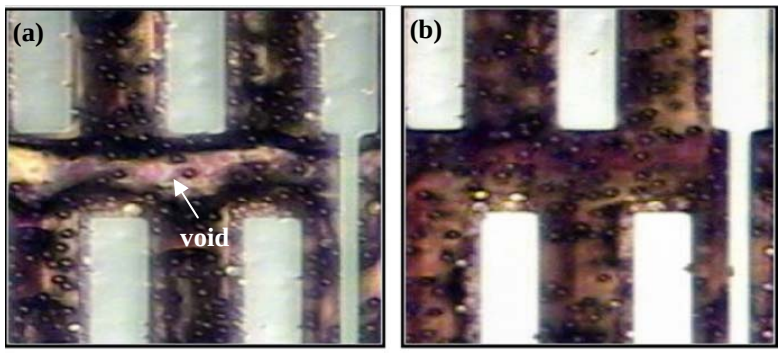
物質之潤濕性(wettability)，若鋼材與膠合物質之潤濕性不佳，易於接合界面形成脫層(delamination)或空孔之缺陷，對接合強度造成不良影響；若兩者具良好之潤濕性，則接合界面完整，不易產生脫層或空孔等缺陷 (如圖九所示) [32]，有助於提升鋼材與膠合物質之接合強度。



(a) Poor wetting　　(b) Good wetting

圖九：鋼材表面與膠合物質之接合界面示意圖，(a)鋼材表面未經電漿活化處理，(b)接合界面經電漿活化處理 [32]。

玻璃覆晶接合製程常被應用於封裝液晶顯示器面板，Lin 等人 [33]指出先前研究結果已成功採用異方性導電膠以玻璃覆晶方式使晶片接合於玻璃基板，由於異方性導電膠與玻璃基板間潤濕性不佳，致使其接合界面產生孔洞缺陷，影響接合品質，故以氬氣/氫氣之混合氣體作為電漿活化氣源，用於玻璃基板表面活化處理，去除玻璃基板表面汙染物，該研究結果顯示採用氬氣/氫氣電漿活化能有效清潔玻璃基板表面，使異方性導電膠與玻璃基板之接合界面孔隙率下降，且進一步選用不同氬氣/氫氣電漿活化參數，發現氬氣/氫氣電漿功率 200 W 時，異方性導電膠與玻璃基板之接合界面孔隙率降至為 0 %，顯示接合界面完整無孔洞缺陷，有效提升其接合強度，如圖十所示 [33]。

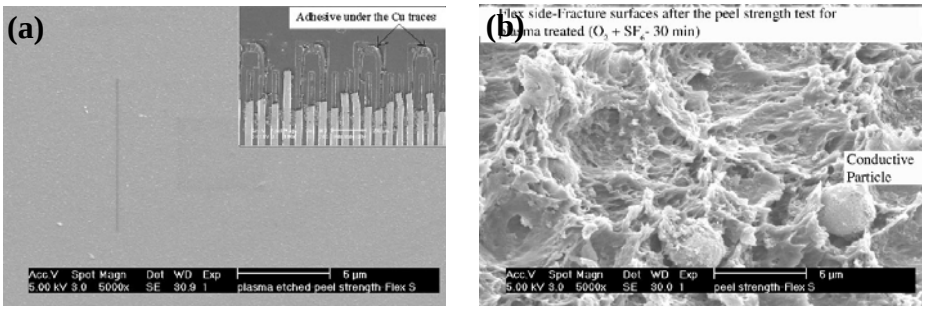


圖十：以不同氬氣/氫氣混合電漿活化處理玻璃基板之接合試片俯視圖，(a)未經電漿活化處理，(b)經電漿功率 200 W 活化處理玻璃基板 [33]。

氬氣電漿常用於晶片金銲墊之表面活化處理，金銲墊表面之污染物主要來源為金銲墊製作過程之殘留物質或晶片以快速膠貼合於導線架後，固化(cured)過程之揮發物沈積於金銲墊表面，以歐傑電子儀(Auger electronic spectroscopy)分析金銲墊表面污染物之主要成分為碳(C)與鎳(Ni)，經氬氣電漿活化處理後，金銲墊表面之碳含量大幅下降，而鎳元素亦降至歐傑電子儀無法偵測之濃度，顯示氬氣電漿有效移除金銲墊表面之污染物，隨後進行金線與金銲墊之熱音波銲線(thermosonic wire bonding)製程，金球可成功接著於經氬氣電漿活化後之金銲墊，且推球試驗(ball-shear test)與拉力試驗(wire-pull test)所得之接合強度均高於未進行電漿活化處理者 [17]。此實驗結果得知電漿活化處理有效除去材料表面之污染物，驗證電漿活化處理之效能。氬氣電漿表面活化技術亦應用於鍍著銀膜銅導線架之活化處理 [34]，經氬離子電漿活化處理後，鍍著銀層與未鍍銀膜裸銅導

線架表面之接觸角(contact angle)均下降，但短時間、小功率之電漿活化處理，效果並不顯著；反之經長時間、高功率之電漿活化處理後，銅導線架表面之接觸角大幅下降，且表面粗糙度低於未經表面活化處理之導線架，證實經電漿表面活化後，可移除材料表面大部分之污染物，且活化後材料表面經元素分析得知表面之碳(C)原子濃度大幅下降，而氧原子(O)之濃度不降反升，顯示以氫氣作為電漿活化氣體，無法順利移除材料表面之氧化膜，故電漿氣體之選擇極為重要。

氫氣電漿活化氣體應用於提升銅導線架(leadframe)與封膠(molding compound)之接合強度(adhesion strength) [35]，實驗結果顯示銅導線架經氫氣電漿活化處理，可使封膠與導線架之接合強度較未電漿活化者提高四倍，配合原子力顯微鏡(atomic force microscope, AFM)觀察經電漿活化與未經電漿活化表面之粗糙度，發現導線架表面之粗糙度與電漿活化時間成正比，導線架表面之粗糙度提高，顯示導線架表面之微凹窩(micro-concave)隨之增加，有助於封膠與導線架接著面積之提升，封膠與導線架之接合界面產生互鎖(interlocking)效應，進而提高導線架與封膠之接著強度。為提升聚乙醯胺(polyimide)軟板與異方性導電膜(ACF)之接合強度，選用三種氣體電漿分別為氫氣、氧氣與氧/SF_6 之混合氣體進行軟性基板之活化處理 [36]，待晶片接著於軟性基板後，以剝離試驗(peel test)檢測晶片與軟性基板之接合強度，驗證三種氣體電漿對軟性基板活化之效用，實驗結果顯示剝離強度與電漿之活化時間成正比，且三種氣體電漿活化後之剝離強度均遠高於未進行電漿活化者，以電子顯微鏡觀察晶片與軟性基板經剝離試驗之破斷面，發現異方性導電膜之表面粗糙度與剝離強度成正比，顯示表面粗糙度越高，非導電膜與軟板之接觸面積越大，異方性導電膜與基板之界面形成互鎖(interlocking)強化機制，如圖十一所示 [36]。三種氣體電漿以氧氣/SF_6 混合氣體活化後之表面粗糙度最大，氧氣電漿次之，氫氣電漿最為平滑；氣體電漿對剝離強度之影響與軟性基板活化後表面粗糙度之改變相符，軟性基板與異方性導電膜之接合強度主要受軟性基板活化後表面粗糙度之影響，軟性基板表面形成越多微凹孔，有助於提升軟性基板與異方性導電膜之接合強度。



圖十一：晶片以異方性導電膠接合軟性基板後之基板側破斷面圖，(a)基板未經 O_2/SF 活化處理，(b)基板未經 O_2/SF 活化處理 [36]。

Cvelbar 等人 [37]以三種方式活化銅膜，分別為濕式化學清潔、氧氣電漿活化與氫氣電漿活化，銅膜經活化處理後，銅膜表面塗佈銀膠，量測銅膜與銀膠接點之導電性。實驗結果顯示三種活化方法均可降低銅膜與銀膠之接點電阻，提高接點之導電性，但三種方法中以氧氣電漿活化後，再以氫氣電漿活化之效果最佳，氧氣電漿可除去銅膜表面之有機物，但銅膜經氧氣電漿活化後，銅膜表面即生成大量氧化膜，而氫氣電漿可與氧化膜產生還原反應之活化效果，因此經氫氣電漿活化後，銅膜表面之氧化膜可被氫氣還原，進而提高銀膠與銅膜之導電性。此一研究充分掌握各種氣體電漿之特質，調整電漿活化順序，可得理想之活化效果。

Koo 等人 [38]選用氫氣與氬氣/氧氣之混合氣體作為電漿活化氣源，用於金凸塊(Au bump)表面之活化處理，該研究結果指出採用氬氣電漿活化金凸塊表面，可獲得良好之清潔結果，且經活化處理後之金凸塊以超音波覆晶製程接著於基板，其接合強度隨電漿活化時間增長而提高，活化時間為一秒時達到最高值。反觀以氬/氧混合氣體作為電漿活化氣源，經活化處理後，金凸塊以相同參數覆晶接合於基板之接合強度遠低於以氬氣電漿活化者，以歐傑電子分析儀分析電漿活化後金凸塊之縱深元素組成(depth profile)，氬氣電漿活化後金凸塊表面碳元素含量大幅降低，且僅存少量之氧原子，而經氬氣/氧氣混合氣體電漿活化之金凸塊，其表面之氧原子含量大幅上升，顯示氧離子電漿與金凸塊表面產生氧化作用，由化學分析儀(ESCA)圖譜分析後，金凸塊表面之氧化物應為 Au_2O_3，此研究結果顯示對不易氧化之金凸塊，亦可能與電漿活化之氧離子產生氧化反應，而生成氧化膜，進而影響其覆晶接合強度。此外，該研究結果也顯示金凸塊之最佳活化狀況，並非隨氬/氧混合氣體電漿活化時間增長而提高，過長的活化時間易造成被清除之污染物在真空艙中，再度污染材料表面，因此電漿活化時間為表面活化處理之重要參數。

綜整上述電漿表面活化處理之相關文獻，電漿活化效能與選擇電漿氣體種類、材料表面特性、活化時間、污染物之組成等具相關性，特別是材料表面污染物之判定，亦為影響選擇電漿氣體之重要因素，而電漿活化之效能影響後續材料接合之品質。就目前公開發表文獻歸納，泛用電漿活化氣源之選擇可分為惰性電漿氬氣、還原性電漿氫氣、氧化性電漿氧氣或採用混合氣源方式進行電漿表面活化處理，而電漿表面活化處理之主要機制為去除接合材料表面之污染物、還原接合材料表面之氧化膜與提高接合材料表面之粗糙度或形成微凹孔，提高接合材料間之接合面積，進而提高其接合品質。由上述文獻可知電漿活化處理有助於材料間接合品質之提升。

4.研究方法

以熱音波植凸塊技術，於晶片上植金凸塊(gold stud bump)，每一晶片含有九個面積陣列之金凸塊，晶片尺寸為 1.197x0.97 (mm^2)，金凸塊接著於晶片銲墊後，均經推球試驗之檢測，確保金凸塊與晶片銲墊之接合強度高於 JEDEC 之標準。實驗選用之軟性基板為銅箔直接塗佈聚乙醯胺，經高溫接著後所得之無膠式單面軟性銅箔基板，銅箔厚度約為 8 μm，聚乙醯胺厚度約為 12 μm。晶片與軟性基板以非導電膠接合之實驗步驟係將非導電膠塗佈於聚乙醯胺表面，再將植金凸塊之晶片反轉，以熱壓覆晶製程接合於軟性基板，主要接合參數為接合溫度100℃、接合負荷 3.5 kgf，持壓 2 min 後，將溫度提升至 200℃，進行非導電膠之固化。

選用物理性氬氣電漿進行軟性基板與晶片金凸塊表面活化之氣源，表面活化過程之底壓與氬氣流量分別固定於 180 mtorr 與 60 sccm，為探討不同電漿活化參數對晶片與電漿晶片與軟性基板接合強度之影響，改變活化時間與功率兩項參數，當功率固定為 400 W 時，活化時間為 10-50 s；當活化時間固定為 30 s，功率為 200-600 W。

軟性基板經氬氣電漿活化處理後，以 ESCA 進行表面元素分析，評估電漿活化製程對接合表面組成之影響；以座滴法量測不同氬氣電漿活化處理後，試片表面之潤濕性；以 AFM 與 FESEM 量測試片表面粗糙度與觀察試片經電漿活化後之表面型態；晶片熱壓覆晶接著於軟性基板後，以剪力試驗(die-shear test)量測其接合剪力值，並以電子顯微鏡(SEM)觀察接合界面之微觀組織與剪力試驗後之破

斷面，搭配能量光譜儀(EDS)分析破斷之元素組成，判斷其破斷模式。

為探討軟性基板經氬氣電漿處理後之活化效能，以電漿功率 400 W、時間 30 s 進行活化後之軟性基板，放置至防潮箱中儲存 0-14 天，再依序與晶片以非導電膠完成熱壓覆晶接合，並以剪力試驗、SEM 及 EDS 觀察接合試片之橫截面與破斷面，比較接合試片剪力值之差異性，進而判斷儲存時間對晶片與軟性基板接合強度與破裂模式之變化，並依實驗結果建議經氬氣電漿活化後試片之有效儲存時間。

5.結果與討論

5.1 非導電膠接合晶片與軟性基板

圖十二(a)所示為晶片以非導電膠與熱壓覆晶製程接著於軟性基板之外觀圖，圖中所示晶片以非導電膠成功接著於軟性基板，進一步將接合試片鑲埋後，研磨其橫截面，如圖十二(b)所示，晶片金凸塊接著於軟性基板表面且金凸塊與軟性基板間無殘留之非導電膠，顯示晶片與軟性基板間形成有效之電訊通路，此一實驗結果說明以適當之熱壓覆晶接合參數(接合溫度 100℃、接合負荷 3.5 kgf，持壓 2 min)，可將塗佈於軟性基板上之非導電膠移除，使金凸塊與軟性基板表面直接接著，形成有效之電訊通路。

5.2 電漿活化對軟板表面性質之影響

5.2.1 電漿活化對軟板表面組成之影響

以 ESCA 分析軟性基板經不同氬氣電漿活化參數處理後，軟性基板表面之元素組成，如圖十三所示，未進行電漿處理之軟性基板表面所含元素為碳(C)、氮(N)與氧(O)，因軟性基板為聚乙醯胺(polyimide)與銅膜組成之雙層結構，而聚乙醯胺(polyimide)之主要組成元素即為碳、氮與氧，此一分析結果與聚乙醯胺之組成元素相符。經氬氣電漿活化處理後之試片，其表面之組成元素與未處理前之試片相同，但經氬氣電漿活化處理之試片，其表面碳含量下降，此一分析結果說明氬氣電漿活化係屬物理性之活化製程，不易對試片表面之組成產生改變，檢視試片經氬氣電漿活化處理與未處理試片表面組成元素之原子百分比，發現經氬氣電漿活化處理試片表面之碳原子較未處理試片為低，而經處理試片之氧原子則些微升高，推論氬氣電漿屬物理性之活化處理，係以高速之氬氣離子轟擊試片表面，可移除試片表面之汙染物，但無法移除試片表面之氧化物，故經活化處理試片表面之碳原子百分比降低且試片表面之氧原子百分比升高，如表一所示。氧原子百分比升高另一可能原因為轟擊過程中，聚乙醯胺之結構斷鍵，產生更多自由基，該自由基再與空氣中的氧鍵結，而使氧原子百分比增加[39]。

為進一步檢視氬氣電漿活化處理是否有效提升軟性基板表面之潔淨度，以座滴法檢測經氬氣電漿活化處理後接觸角之變化，如圖十四所示，未經氬氣電漿活化處理試片之接觸角約為 70°，如圖十四(a)所示，而軟性基板經氬氣電漿功率 400 W 與活化時間 30 s 處理後，試片表面之接觸角降至 6.52°，如圖十四(b)所示，此一實驗結果驗證氬氣電漿活化處理確實可移除基板表面之汙染物，進而提高軟性基板表面之潤濕性，氬氣電漿功率固定於 400 W，不同活化時間下，軟性基板表面之接觸角隨活化時間增加而下降，且於活化時間 20 s 後達到最低值 4.19°，隨活化時間增加至 50 s，接觸角呈小幅度之變化，亦即軟性基板表面之潤濕性維持一穩定值，如圖十五所示；若氬氣電漿之活化時間固定於 30 s，不同電漿功率下進行軟性基板之活化處理，軟性基板表面之接觸角隨電漿活化功率之增加而下降，電漿功率由 200 W 提升至 600 W，試片表面之接觸角並無明顯變化，隨電漿活化

功率增加而小幅度改變，顯示軟性基板表面之潤濕性維持於穩定區間，如圖十五所示。此一實驗結果與前述以化學分析儀(ESCA)分析軟性基板表面經氬氣電漿活化處理後，試片表面組成之結果一致，再度驗證以氬氣電漿對軟性基板表面進行活化，可除去基板表面之汙染物，進而提高基板表面之潔淨度。

5.2.2 電漿活化對基板表面粗糙度之影響

圖十六所示為軟性基板經氬氣電漿於不同活化時間(活化功率固定為 400 W)與不同活化功率(活化時間 30 s)處理後，軟性基板表面平均粗糙度之關係圖，可知未進行電漿活化軟性基板表面之粗糙度值為最高，達 197 nm，隨著氬氣電漿於不同活化時間與不同活化功率處理後，其表面粗糙度均較未處理試片為低，但隨活化功率增至 600 W 或延長活化時間至 50 s，均可發現試片表面粗糙度隨之上升趨勢，推論其原因為氬氣電漿係屬物理性之活化，以氬氣離子高速轟擊試片表面，試片表面污染物隨之除去，但延長活化時間或提升氬氣電漿功率均可能移除軟性基板表面材料，故其表面之粗糙度上升，此一實驗結果亦說明過高氬氣電漿活化功率或過長活化時間均可能造成試片表面之粗糙化。圖十七所示為軟性基板表面未經氬氣電漿活化處理與經活化處理後之表面粗糙度形態圖，未經氬氣電漿活化試片表面粗糙度之形態高低差異較大，如圖十七(a)所示，相較於未經氬氣電漿活化處理試片表面粗糙度之形態，經氬氣電漿於功率 400 W 與活化時間 30 s 活化後之粗糙度形態呈現較為圓滑且出現較多微小凹窩(dinple)，如圖十七(b)所示，該圓滑形態應為氬氣電漿去除試片表面污染物所致。進一步以較高倍率之電子顯微鏡觀察軟性基板未經活化處理與經活化處理後之表面形態(surface morphology)，如圖十八(a)、(b)所示，相較未處理與經活化處理試片之表面形態，發現經氬氣電漿處理後軟性基板表面較平整且汙染物亦較少，顯示電漿處理確實能有效清除表面雜質，提高軟性基板表面之潔淨度。

5.2.3 氬氣電漿活化對試片剪切強度之影響

圖十九為軟性基板經不同氬氣電漿活化時間與功率處理後，以剪力試驗測得晶片以非導電膠熱壓接著於軟性基板之剪力值，晶片與軟性基板皆未進行氬氣電漿處理之接合試片剪力值約為 3.25 kgf，經氬氣電漿處理之接合試片，其剪力值皆大於未經氬氣電漿處理之接合試片，相較不同活化時間與不同氬氣電漿功率下，可清楚發現氬氣電漿功率 400 W 與活化時間 30 s 時，其剪力值達最高值 4.24 kgf，較未經氬氣電漿活化處理接合試片之剪力值提升約 30.5 %，此一結果驗證氬氣電漿活化處理確實可提升晶片以非導電膠熱壓接著軟性基板之接合強度，當活化時間延長至 50 s 或電漿功率提升到 600 W 時，其剪力值分別下降至 3.77 kgf 與 3.98 kgf，推論其原因為過多能量或活化時間使較為平整之試片表面再度因氬氣離子轟擊而過度產生較為粗糙形貌，如圖十六所示，致使接合晶片與軟性基板兩側之非導電膠量減少，使其晶片與軟性基板接合試片之剪力值下降，為驗證粗糙度對剪力值之影響，觀察晶片與基板端旁之膠量高度，發現未經電漿活化試片之高度最低，其次為軟性基板經氬氣電漿功率 600 W 活化之接合試片，最高則為軟性基板經氬氣電漿功率 400 W 活化之接合試片，如圖二十所示。

進一步探討氬氣電漿活化對晶片與軟性基板接合界面之影響，觀察晶片與軟性基板接合試片之橫截面，如圖二十一所示，未經電漿活化之接合試片，金凸塊與非導電膠間及非導電膠與軟性板表面間，均可發現脫層(delamination)與孔洞之缺陷，如圖二十一(a)所示，此一觀察結果亦可說明未經氬氣電漿活化處理試片之接合強度較低(圖十九)，而經過氬氣電漿活化處理後試片之接合界面完整，非導電膠與軟板表面間則無脫層缺陷，但因晶片端之金凸塊未經過電漿活化處理，

故金凸塊與非導電膠間仍存在孔洞缺陷，如圖二十一(b)所示。

為驗證改變氫氣電漿活化時間與電漿活化功率對剪力值之影響，觀察接合試片經剪力測試後之破斷面，如圖二十二所示，未經氫氣電漿活化之接合試片經剪力測試後，大部分非導電膠皆殘留於晶片端，如圖二十二(a)所示，而基板端僅殘留少量之非導電膠，如圖二十二(b)所示，該斷裂模式應為非導電膠與軟性基板之接合界面產生剝離(peel-off)，此一結果亦說明非導電膠與未經活化處理軟性基板間之接合性不佳；隨著軟性基板進行電漿處理後，晶片與軟性基板接合試片經剪力測試後之破斷表面形態如圖二十二(c)及圖二十二(d)所示，非導電膠殘留於晶片端與軟性基板表面，因軟性基板經氫氣電漿活化處理後，非導電膠與軟性基板表面之潤濕性較佳，剪力試驗時，斷裂發生於固化之非導電膠，此一結果驗證非導電膠與軟性基板間具較佳之接合強度；圖二十二(e)與圖二十二(f)顯示部分非導電膠殘留於晶片端及基板端，但殘留於晶片端之非導電膠較多，顯示其接合強度雖較未經氫氣電漿活化接合試片(圖二十二(a)與圖二十二(b))高，但較軟性基板經電漿活化功率 400 W(圖二十二(c)與圖二十二(d))之接合強度低，此一觀察結果與剪力強度之測試結果一致。

由晶片與軟性基板接合試片之剪力測試結果得知氫氣電漿活化對軟性基板確實能改善晶片與軟性基板之接合試片剪力強度，為消除金凸塊與非導電膠間之孔洞缺陷(圖二十一(a)與圖二十一(b))，將晶片固定以氫氣電漿功率 400W、活化時間 30s 之參數活化與軟性基板均進行不同氫氣電漿活化處理後，再以非導電膠進行接合，以剪力試驗測得晶片以非導電膠熱壓接著於軟性基板之剪力值，如圖二十三所示，晶片與軟性基板均進行氫氣電漿活化處理之試片剪力值皆高於僅基板端進行氫氣電漿活化處理之試片剪力值，並呈現相似趨勢 (圖十九) ，於晶片與軟性基板之氫氣電漿功率 400 W、活化時間 30 s 時，剪力值達到 5.89 kgf 為最高值，與僅基板端進行氫氣電漿功率 400 W、活化時間 30 s 之試片剪力值(4.24 kgf)相比，提升約 28%，推論其原因為晶片金凸塊受氫氣電漿活化處理能提升表面之潤濕性，促使晶片與軟性基板在進行接合時提高金凸塊與非導電膠之接著，進而提升其剪力強度。隨著軟性基板之氫氣電漿功率增加至 600 W 或活化時間延長到 50 s (晶片端依然固定電漿功率 400 W、活化時間 30 s)，接合試片之剪力值下降至 4.56 kgf 及 5.39 kgf，推論原因與上述軟性基板表面粗糙度所述相同(圖十六、圖二十)。

進一步驗證金凸塊因氫氣電漿處理而提升其潤濕性使剪力強度增加之推論，觀察晶片與軟性基板進行不同氫氣電漿時間與功率之接合試片橫截面之接合界面，如圖二十四所示，基板端未進行氫氣電漿活化(晶片端電漿功率 400 W、活化時間 30 s)之試片接合界面，如圖二十四(a)所示，非導電膠與軟性基板間有脫層及空洞缺陷，而金凸塊與非導電膠間則接著良好，說明此試片之剪力值高於晶片與軟性基板均未進行氫氣電漿之試片剪力值(圖二十一(a))。圖二十四(b)顯示晶片與軟性基板均進行氫氣電漿活化處理，故可觀察到非導電膠與軟性基板間以及金凸塊與非導電膠皆接著完整，無孔洞、脫層之缺陷，此情形亦與圖二十四(c)相似，顯示晶片與軟性基板均進行氫氣電漿處理，確實提升接合試片之剪力值，符合剪力測試實驗結果(圖二十三)。

為證實晶片端進行氫氣電漿活化處理對剪力值之影響，分析晶片與軟性基板經不同氫氣電漿活化處理之接合試片經剪力試驗後之破斷面，如圖二十五所示，圖二十五(a)、(b)顯示基板端未進行氫氣電漿處理，故試片之斷裂模式為大部分非導電膠由軟性基板與非導電膠間剝離進而殘留於晶片端上，與圖二十二(a)、(b)

相似，晶片與軟性基板接合之剪力值，主要來自非導電膠與軟性基板間之接著強度，故非導電膠與軟性基板之接著力較差，晶片與軟性基板之剪力值隨之降低(如圖二十四所示)。當晶片與軟性基板同時進行氬氣電漿活化處理(氬氣電漿功率為 400 W、活化時間 30 s)，其接合試片經剪力測試後之斷面如圖二十五(c)、(d)所示，其破斷面型態明顯與圖二十二 (c)、(d)有所差異，進一步藉由 EDS 分析晶片端與基板端之破斷面元素組成，可得圖二十六(a)之元素分別為碳(C)、鋁(Al)、銅(Cu)，推論 point 1 為用以固定軟性基板之鋁載板，如圖十二(a)所示，軟性基板之雙層結構為聚乙醯胺及銅箔，顯示圖二十五(d)所示之凹槽為聚乙醯胺與銅層於剪力試驗過程中產生破裂，軟性基板兩層之材料均破裂轉移至晶片端，而於軟板端出現鋁載板，故分析結果出現鋁(Al)之元素。進一步透過 OM 分析，如圖二十七所示，亦可觀察到 point 1 的位置所呈現出的為鋁(Al)之銀色色澤。point 2 所測得之元素成分主要為碳(C)、氧(O)，如圖二十六(b)所示，顯示 point 2 為聚乙醯胺，由於聚乙醯胺之結構為碳(C)、氧(O)、氮(N)之緣故(圖十三)。而 point 3 之元素組成為碳(C)、氧(O)、矽(Si)、金(Au)，判斷為非導電膠之成分，其中含有微量金(Au)元素，係由於試片鍍金所導致。綜整所述，可判斷晶片與軟性基板經氬氣電漿功率 400 W、活化時間 30 s 後之接合試片之破斷機制，為晶片端上凸塊經氬氣電漿活化處理後，提升軟性基板表面之潔淨度及潤濕性，促使金凸塊與非導電膠間產生良好接著，且此參數對於非導電膠與軟性基板間之接著性能達到最佳狀態，如圖二十二(c)、(d)所示，故進行剪力試驗時，非導電膠抵抗被剝離之力量增加，其強度更將軟板撕裂，致使被撕裂之軟板周圍的部分非導電膠發生斷裂，殘留於晶片端上，而少許金凸塊則由晶片端被剝離至基板端。基板端經氬氣電漿功率 400 W、活化時間 50 s 處理後之接合試片破斷面，由於能量過多導致軟性基板表面產生粗糙度之緣故(圖十六)，使接合試片進行剪力試驗時，其斷裂模式為晶片與非導電膠由軟性基板表面產生剝離，致使大部分非導電膠殘留於晶片端，如圖二十五(e)、(f)所示，與其剪力測試(圖二十三)之趨勢相符。

綜整上述實驗結果，晶片與軟性基板均經氬氣電漿活化處理後，其接合試片之接合界面完整且未發現脫層與空孔等缺陷，說明氬氣電漿活化技術可去除金凸塊與軟性基板表面之污染物，得到潔淨之接合表面，試片之接合界面未存在脫層或空孔等缺陷，且試片破斷面之斷裂模式發生於固化之非導電膠處，晶片與軟板表面均殘留固化之非導電膠，顯示晶片以非導電膠接合軟性基板試片之剪力強度因此而提升。

5.3 儲存時間對軟性基板表面活化效能之影響

由於電漿活化處理表面具時效性，為探討軟性基板經氬氣電漿活化後之儲存時間對於軟性基板表面性質之影響，採用經氬氣電漿處理功率 400 W、活化時間 30 s 之晶片端與不同儲存時間之軟性基板進行接合，軟性基板進行接合前，放置於防潮箱中儲存 0 天~14 天，藉以比較其差異性，接合後試片再由剪力試驗檢測接合試片之剪力值，如圖二十八所示，得知軟性基板經氬氣電漿活化處理後，於 1 天內(小於 24 小時)與晶片進行接合，其剪力強度可達到 5.67 kgf，但隨著儲存時間之增加而下降，當儲存時間為 5 天後時，接合試片之剪力強度降低至 4.12-4.15 kgf 區間，顯示軟性基板放置於大氣中，會逐漸降低軟性基板表面之活化效能及潤濕性，進而恢復為原先未進行氬氣電漿活化處理之狀態。此外，無論儲存時間放置多久(0~14 天)，晶片與軟性基板接合試片之剪力強度仍高於軟性基板未進行氬氣電漿活化者。

為驗證增長軟性基板儲存時間而降低其表面活化效能，進一步觀察晶片與軟

性基板接合試片之橫截面，如圖二十九所示，可發現到軟性基板與非導電膠間以及金凸塊與非導電膠間之接合界面皆完整接著，無脫層或孔洞缺陷，此原因為軟性基板與晶片經氬氣電漿活化處理後，短時間內軟性基板表面仍保有其較佳潔淨度與潤濕性，可使晶片與軟性基板間形成良好接合，如圖二十九(a)所示。軟性基板經儲存五天後與晶片進行接合，可觀察到非導電膠與軟性基板間之接合界面存在些許微小孔洞，由於電漿活化之功效逐漸降低之緣故，導致軟性基板潤濕性不佳而與非導電膠間產生孔洞之缺陷，如圖二十九(b)所示。晶片與儲存 14 天之軟性基板以非導電膠接合，其接合試片發現除了軟性基板與非導電膠間之接合界面殘留孔洞缺陷外，金凸塊與非導電膠間亦存在脫層或孔洞之情形，顯示金凸塊經氬氣電漿活化處理後亦與軟性基板相同，均隨著儲存時間增加而逐漸降低表面活化功效情形，但相較於軟性基板未經氬氣電漿活化處理(圖二十一(a)、二十四(a))而言，軟性基板與非導電膠間之接合界面孔洞皆小於軟性基板未經氬氣電漿活化處理者，顯示雖然軟性基板進行氬氣電漿活化處理後，由於儲存時間原故可能降低軟性基板表面效能，但仍保有電漿活化清潔表面之功效，因此接合試片之剪力值仍高於軟性基板未進行氬氣電漿活化處理及晶片與軟性基板皆未進行氬氣電漿活化處理之試片剪力值。

進一步探討晶片與軟性基板之接合試片破斷面，如圖三十所示，軟性基板經儲存 5 天及 14 天後，接合試片之破斷模式由非導電膠均殘留於晶片端與基板端(圖三十(a)、(b))轉變為大部分非導電膠從軟性基板表面被剝離至晶片端，顯示非導電膠與軟性基板間之接著性下降，如圖三十(a)、(b)所示，圖三十(c)、(d)亦有相似情形，搭配 EDS 分析接合試片破斷面之元素組成，如圖三十一所示，point 4 之元素成分主要為碳(C)、氧(O)、矽(Si)，為固化之非導電膠所產生之孔洞，由於軟性基板表面潤濕性不佳導致非導電膠於熱壓覆晶接合製程中固化不完全，因而降低非導電膠與軟性基板之接著，使接合試片之剪力值下降(圖二十八)。

歸納上述討論結果，晶片與軟性基板之最佳接合時機為經氬氣電漿活化處理後短時間內(小於一天)即進行晶片與軟性基板之接合；隨著軟性基板儲存時間增加，軟性基板及晶片亦逐漸降低其表面活化效能致使接合試片之剪力值下降，但晶片與軟性基板經氬氣電漿活化處理之接合試片，其剪力值仍高於未進行氬氣電漿活化處理者。

6.結論

選用適當熱壓參數下，晶片成功以非導電膠接著於軟性基板，且晶片金凸塊與軟性基板直接接著，形成良好之電訊通路。氬氣電漿活化技術可有效提升晶片以非導電膠熱壓接合於軟性基板之剪力值，其主要之活化機制為氬氣電漿轟擊軟性基板表面，以氬氣離子之高速動能除去軟性基板表面之汙染物，提高軟性基板表面之潔淨度，非導電膠與軟性基板之潤濕性因此隨之提升，進而提高非導電膠與軟性基板界面之接合強度。此外，經氬氣電漿活化後軟性基板之表面粗糙度下降，可得較為平滑之接合界面，該界面有助於提升非導電膠與軟性基板之接合面積，故接合試片之剪力值上升，但若延長氬氣電漿活化時間或提高電漿活化功率，均可使軟性基板表面粗糙度隨之上升，致使晶片與軟性基板之剪力值隨之下降。

由晶片與軟性基板接合試片之橫截面觀察得知軟性基板經氬氣電漿活化處理後之試片，非導電膠與軟性基板之接合界面完整，但凸塊與非導電膠間存在脫層或孔洞等缺陷，若以晶片與軟性基板經氬氣電漿處理後之接合試片，則進一步改善凸塊與非導電膠間之缺陷，使接合試片之整體接合界面完整，更加提升接合試片之剪力值。觀察晶片與軟性基板經氬氣電漿活化處理後接合試片之破斷面，

其斷裂位置發生於固化之非導電膠，顯示非導電膠與軟性基板之接合強度大於非導電膠之固化強度，相較於未經活化處理者，斷裂發生於非導電膠與軟性基板之接合界面，顯示其接合強度不佳。此外，探討軟性基板經氫氣電漿處理後之活化效能時間對接合試片剪力值之影響，結果為軟性基板經氫氣電漿處理後之表面活化效能隨時間增加而降低，進而使接合試片剪力值下降，故建議軟性基板經氫氣電漿處理後與晶片之接合，應於一天內完成可得較佳之接合品質。本研究結果證實以氫氣電漿表面活化技術可改善基板表面之物理特性，提高非導電膠與軟性基板間之接合強度。

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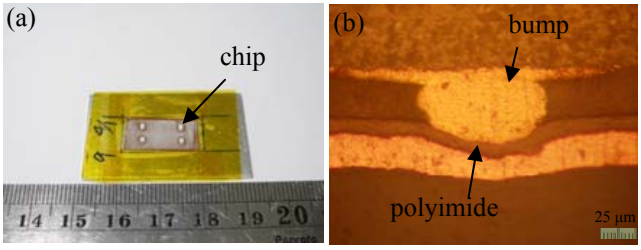
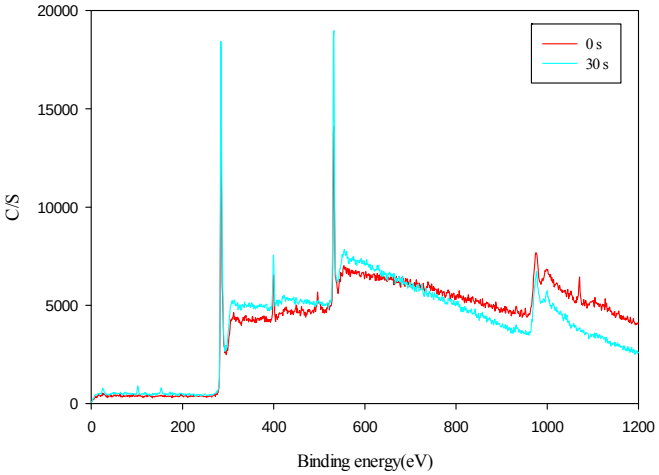
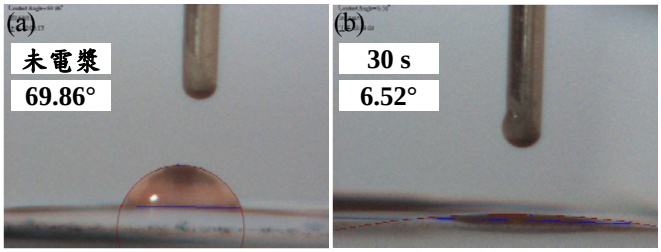
8.圖表



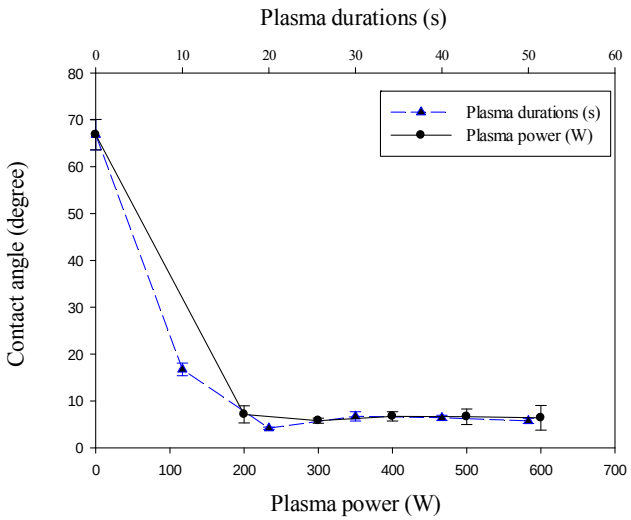
圖十二 以非導電膠與熱壓覆晶製程接合晶片與軟性基板之試片，(a)巨觀圖，(b)橫截面。



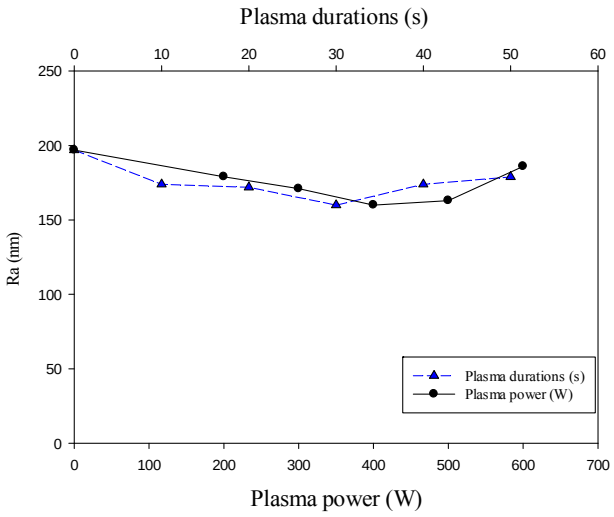
圖十三 以 ESCA 分析軟性基板表面元素組成之全譜圖。



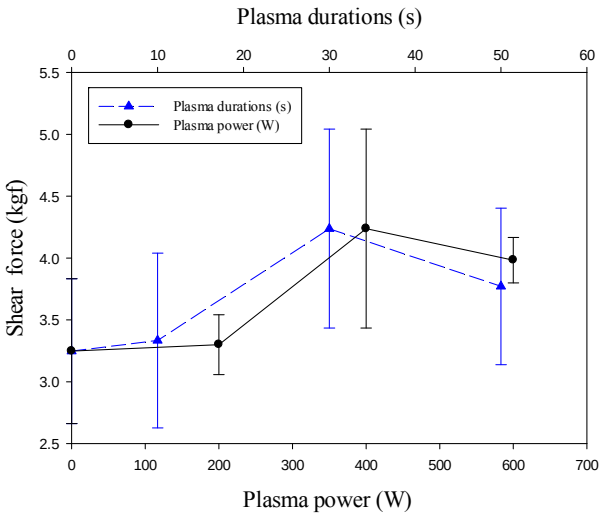
圖十四 軟板基板表面之接觸角測試圖，(a)未經氫氣電漿活化處理，(b) 活化時間 30 s、功率 400 W。



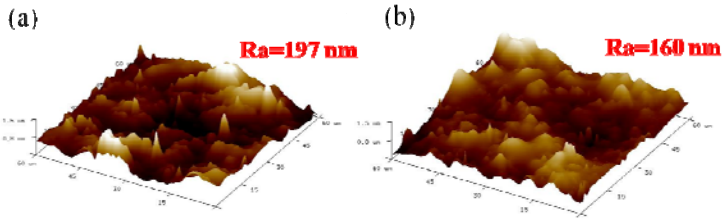
圖十五 不同氫氣電漿活化參數處理與軟性基板表面平均接觸角之關係圖 。



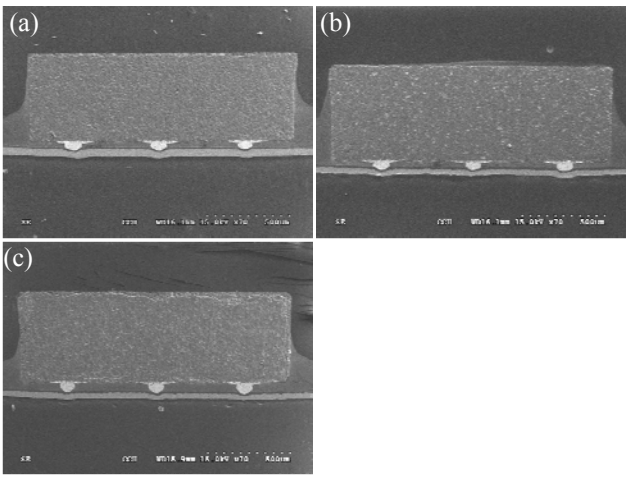
圖十六 不同氫氣電漿活化參數處理與軟性基板表面平均粗糙度之關係圖。



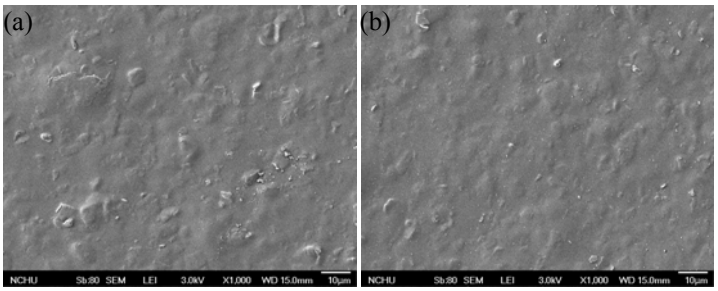
圖十九不同氫氣電漿活化參數處理與試片剪切強度關係圖。



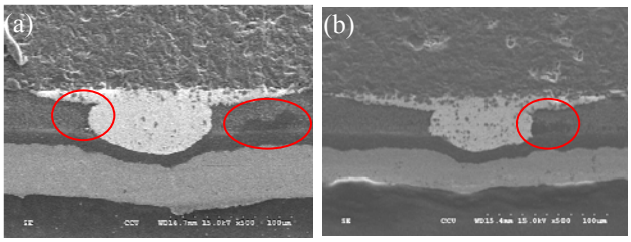
圖十七 軟性基板表面粗糙度形態圖，(a) 未經氫氣電漿活化處理，(b) 活化時間 30 s、功率 400 W。



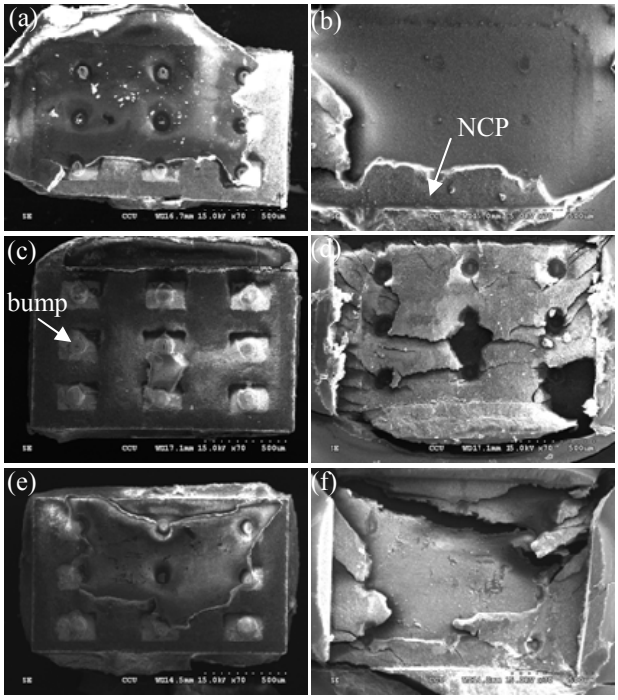
圖二十 晶片與軟性基板接合試片之橫截面，(a) 未經氫氣電漿活化處理，(b) 活化時間 30 s、功率 400 W，(c) 功率 600 W。



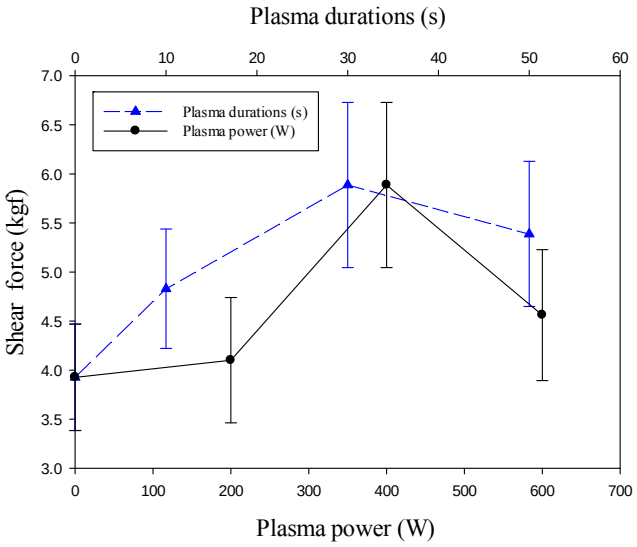
圖十八 軟性基板表面形態之 FESEM 圖，(a) 未經氫氣電漿活化處理，(b) 活化時間 30 s、功率 400 W。



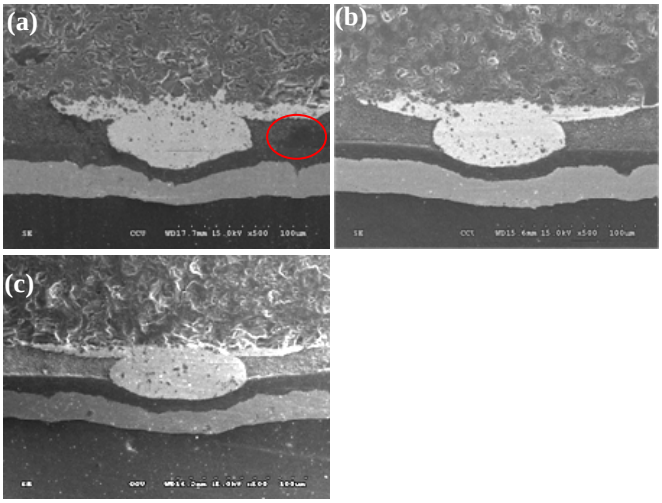
圖二十一 晶片與軟性基板接合試片橫截面之接合界面，(a)晶片端與基板端未經氫氣電漿活化處理，(b)僅基板端電漿活化時間 30 s 、功率 400 W。



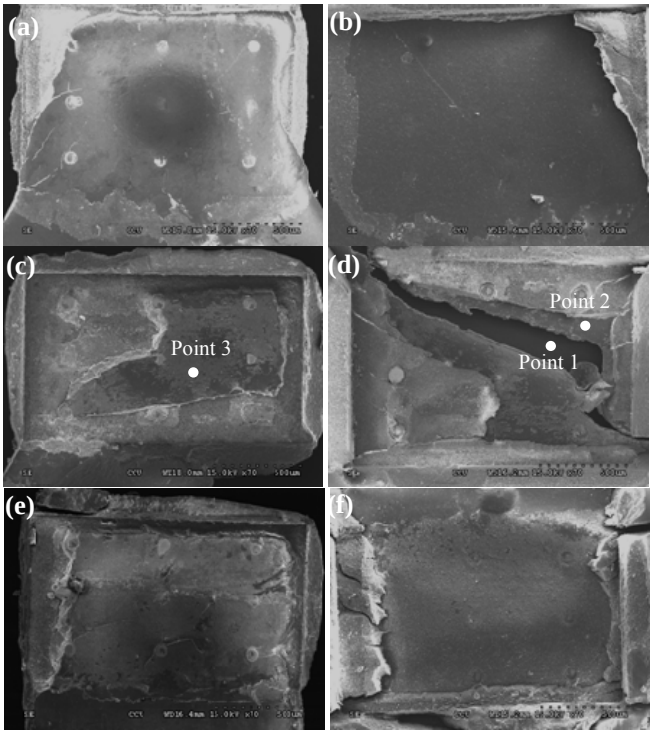
圖二十二 晶片與軟性基板接合試片之破斷面，(a) 未經氫氣電漿活化處理之晶片端，(b) 未經氫氣電漿活化處理之基板端，(c) 活化時間 30 s、功率 400 W 之晶片端，(d) 活化時間 30 s、功率 400 W 之基板端，(e)功率 600 W 之晶片端，(f)功率 600 W 之基板端。



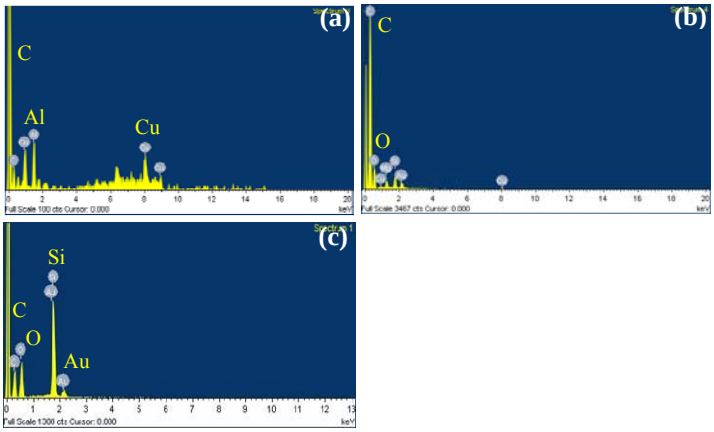
圖二十三 晶片與軟性基板進行不同氫氣電漿活化參數處理與試片剪切強度趨勢圖。



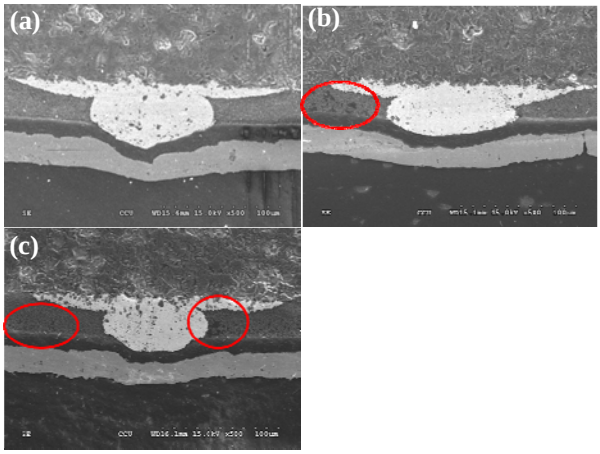
圖二十四 晶片與軟性基板以不同氫氣電漿活化參數處理之試片橫截面之接合界面，(a)僅基板端未經氫氣電漿活化處理，(b)晶片端與基板端均電漿活化時間 30 s 、功率 400 W，(c)基板端電漿活化時間 30s、功率 600 W。



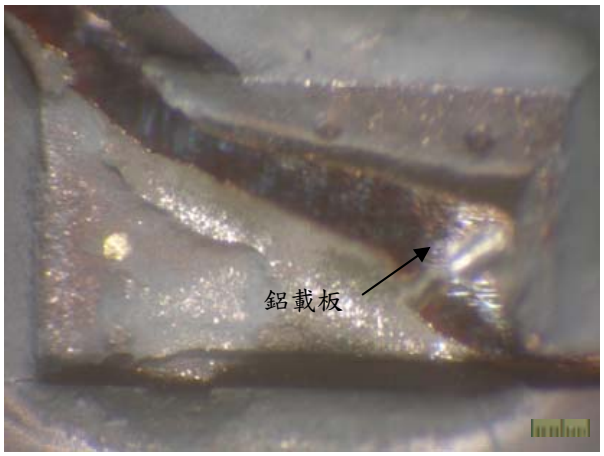
圖二十五 晶片與軟性基板接合試片之破斷面，(a)經氫氣電漿處理活化時間 30 s、功率 400 W 之晶片端，(b)未經氫氣電漿活化處理之基板端，(c)活化時間 30 s、功率 400 W 之晶片端，(d) 活化時間 30 s、功率 400 W 之基板端，(e)活化時間 30 s、功率 400 W 之晶片端，(f)活化時間 30 s、功率 600 W 之基板端。



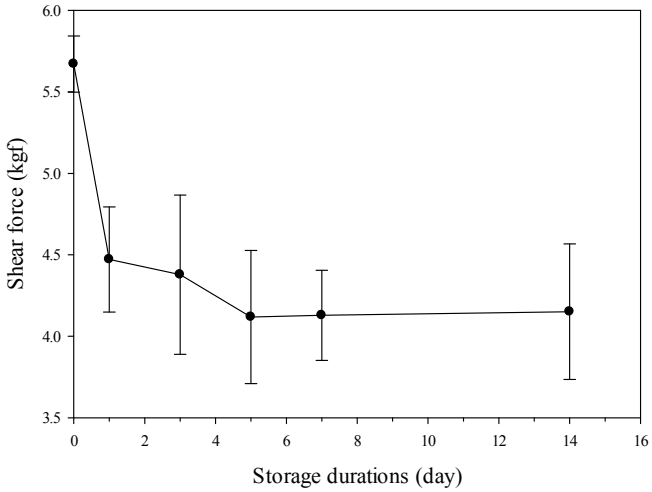
圖二十六 晶片端與基板端均經氫氣電漿活化時間 30 s、功率 400 W 之接合試片破斷面 EDS 分析，(a)point 1 之分析圖譜，(b) point 2 之分析圖譜，(c)point 3 之分析圖譜。



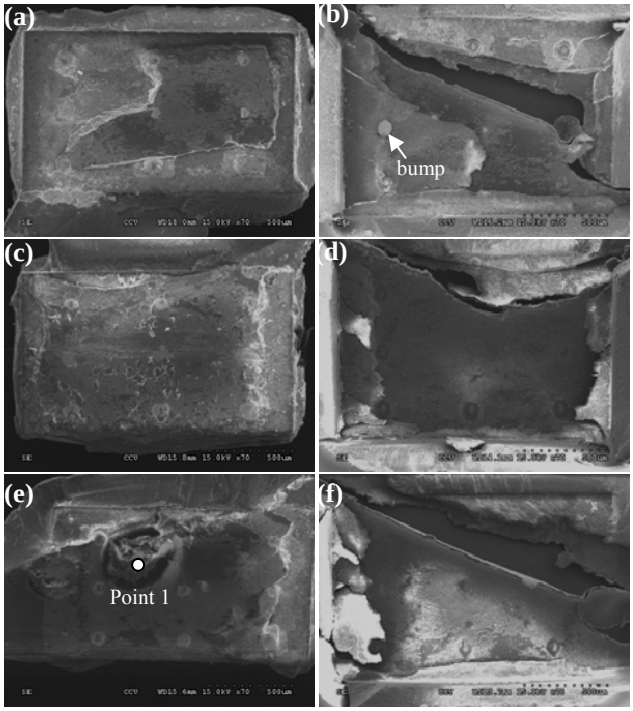
圖二十九 晶片與軟性基板接合試片之橫截面之接合界面，(a)儲存時間 0 天，(b)儲存時間 5 天，(c)儲存時間 14 天。



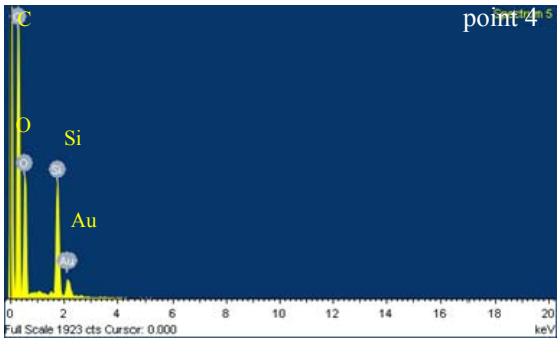
圖二十七 晶片端與基板端均經氫氣電漿活化時間 30 s、功率 400 W 之接合試片破斷面之基板端 OM 圖。



圖二十八 軟性基板經氫氣電漿處理活化時間 30 s、400 W 後之儲存時間與接合試片剪切強度趨勢圖。



圖三十 晶片與軟性基板均經氫氣電漿處理活化 30 s、400 W 之接合試片破斷面，(a)軟性基板儲存 0 天之晶片端，(b) 軟性基板儲存 0 天之基板端，(c) 軟性基板儲存 5 天之晶片端，(d) 軟性基板儲存 5 天之基板端，(e) 軟性基板儲存 14 天之晶片端，(f) 軟性基板儲存 14 天之基板端。



圖三十一 軟性基板儲存 14 天之接合試片破斷面之 EDS 分析圖譜。

表一 以 ESCA 分析軟性基板未經氫氣表面活化與經表面活化後表面之組成元素原子百分比

Plasma treatment / Elements (at %)	Without	30 s、400 W
C	76.2	73.1
O	17.7	21.2
N	6.1	5.6

國科會補助專題研究計畫出席國際學術會議心得報告

日期：103 年 9 月 3 日

計畫編號	MOST-102-2221-E-040-005		
計畫名稱	以表面活化技術提高非導電膠接合矽晶片與軟性基板之接合強度與可靠度		
出國人員姓名	莊正利	服務機構及職稱	中山醫學大學、教授
會議時間	103 年 8 月 12 日至 103 年 8 月 15 日	會議地點	中國、成都
會議名稱	(中文)2014 年電子封裝技術國際會議 (英文)2014 International Conference on Electronic Packaging Technology (2014 ICEPT)		
發表題目	(中文)氬氣電漿提升晶片與基板之覆晶接合強度 (英文) Increasing Bonding Strength of Chips and Substrates Assembly by Argon Plasma		

一、參加會議經過

此一電子構裝國際會議已持續舉辦 15 年,每年吸引眾多大陸地區與國際專業人士參與會議，已成為國際大型電子構裝會議之一，會議舉辦地點亦從過去沿海高度發展地區轉移至內陸地區，今年舉辦地點為四川省成都市，並由成都市之中國電子科技大學(UESTC)承辦會議相關工作。議程由 8 月 12 日至 15 日共四天，會議第一天舉辦教育訓練課程，講師涵蓋中外學術界與產業界師資，第二天邀請墊子構裝各領域傑出學者或業界人士演講，講題涵蓋電子構裝未來發展、3-D 電子構裝與可靠度測試、分析等相關主題，第三天進行各分組論文發表，第四天則安排成都市自由行，會場提供不同旅遊路線，可視自我需求，購買票卷，參與旅遊。本年度會議投稿主題可分為先進構裝(advance packaging)、系統整合(system integration)、構裝材料與製程(packaging materials and process)、構裝設計與模擬(packaging design and modeling)、內導線技術(interconnect technologies)、先進製造與封裝設備(advanced manufacturing and packaging equipment)、品質與可靠度(quality and reliability)、微波與功率電子封裝(microwave and power electronics packaging)、固態照明封裝(solid state packaging)與新興技術(emerging technologies)，分類較往年更為精細與多元。

會議中邀請多位重量級電子構裝研究學者，如 William T. Chen、Wilmer R. Bottoms 與 John H. Lau 等,其中 John H. Lau 在演講中明確指出電子構裝應依不同產品運用平台之需求，慎選適當之構裝製程，決定電子構裝製程之主要因子為成本(cost)、電子產品之尺寸與重量(size and weight)、電子產品對性能(performance)要求度與可靠(reliability)等。針對大眾化消費型電子產品應以封裝製程成本為其首要考量要點；對電腦或網路通訊元件則應先考慮電子元件之性能；交通與軍事用途之電子元件則須同時考量性能與可靠度，所以現今產業界熱門 3-D 封裝製程未必符合各種電子元件構裝之需求。此外，在演講中

展示目前國際知名廠家於 3-D 電子構裝之發展，如 Amkor 採用晶片直接堆疊後，以銅銲線製程(Cu wire bonding process)完成堆疊晶片與基板 I/O 之電訊通路連接，蘋果公司 A7 處理器亦採用 3- D 封裝設計，同時採用熱音波銲線製程(thermosonic wire bonding process)與錫凸塊(Sn bump)完成堆疊晶片與基板之訊號連結，台積電則以錫球(Sn ball)與銅凸塊(Cu bump)覆晶接合並結合 TSV 製程完成 3-D 封裝。綜觀各家廠商所發表 3-D 電子構裝設計，各有其優缺點與電子產品不同運用平台，再次說明產品應用需求不同，其封裝設計與製程之選擇意有所不同。

二、與會心得

今年是第三次參與此一國際會議，會議組織與會務運作均較過去純熟，會議舉辦地點亦由過去校園轉變成飯店會議中心，更結合中國各大具特色都市輪流舉辦，不僅舉辦會議品質優化，吸引更多國際專業人士參與，讓此一會議更形龐大。會議論文主題區分更加詳細，對整個電子構裝專業領域更顯完整，投稿篇數均較往年增加。此外，觀察中國在電子構裝技術之發展趨勢，學界與業界發展之技術水平已不下於台灣，相較於台灣學界對電子封裝領域之研究更顯興盛，會議中與哈爾濱工業大學及上海大學與會教授聊及電子封裝學術發展趨勢與該校主要研究題目，發現中國採取團隊式研究模式，一位正教授帶領數位教授、副教授或助理教授與講師共同指導研究生，進行較大範圍之研究，整個研究團隊涵蓋各種領域之教師，例如哈爾濱大學工業大學電子構裝團隊包含材料、熱傳、應力分析、可靠度等專長教師，因此可進行電子元件之整體研究，更可接受業界委託開發電子元件之構裝技術，包含製程設計、材料選擇、應力分析與可靠度分析，完整建構電子元件之封裝技術，亦可取得較佳之研究資源與設備。此一發展模式實為國內學界研究可參考方式。

由投稿文章方向或與會學者專家之演講內容得知立體化封裝已成電子構裝之研究主流，但晶片立體化封裝製程須結合良好定位系統與高度精密機械方可完成，然而晶片堆疊之精密機械價格昂貴，非單一學術機構具備之採購能力，顯然該技術之發展有賴於產、官界於經費或設備之支持，方可進行相關技術之研究與探討，此次參與會議後，深深覺得與電子封裝產業之密切交流，以取得相關研究設備之支持或由政府設立相關研究中心，採購共同研究設備供國內學者進行研究使用，降低實驗設備之技術瓶頸，顯然已成此一領域發展必行之趨勢。

三、發表論文全文或摘要

Abstract

The plasma surface activation was applied to the thermal-compression bonding of chips and substrates. An Ar gas was selected to perform the physical plasma treatment on the bonding surface of Au bumps and Cu electrodes. This plasma-activated technology was expected to remove the surface contaminants, and then to reduce the bonding barrier for chips and substrates assembly. The experimental results presented an effective improvement in the die-shear force performance of chips and substrates assembly using the Ar plasma activation. Increasing the die-shear force was attributed to remove the contaminants on the surface of Cu electrodes and Au bumps by the Ar plasma activation. After Au bumps and Cu electrodes were activated by Ar plasma, neither delamination nor crack is found at bonding interface between Au bumps and Cu electrodes for chips and substrates assembly. The die-shear forces were higher than the minimum required value stated in the JEDEC specifications for Cu electrodes and Au bumps with Ar plasma activated. As Cu electrodes with Ar plasma treating under various activated durations, the fracture mode of Au bumps separating from the surface of Cu electrodes transforms to that of Au bumps separating from the bond pads, indicating the bonding strength of Au bumps and Cu electrodes is higher than that of

Au bumps and bond pads. A low contact angle was also determined on the surface of Cu electrodes after the Ar plasma activated, indicating a clean bonding surface was achieved. A clear atomic interdiffusion between Au bumps and Cu electrodes was observed for Au bumps and Cu electrodes with Ar plasma activated. The Ar plasma activation was an effective scheme to improve the bonding strength of chips and substrates assembly. Thus, the Ar plasma activation has great potential to be applied to chips and substrates assembly.

Keywords—argon plasma activation, thermal compression bonding, copper electrode, gold bump.

論文全文：

Increasing Bonding Strength of Chips and Substrates Assembly by Argon Plasma

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Abstract—**The plasma surface activation was applied to the thermal-compression bonding of chips and substrates. An Ar gas was selected to perform the physical plasma treatment on the bonding surface of Au bumps and Cu electrodes. This plasma-activated technology was expected to remove the surface contaminants, and then to reduce the bonding barrier for chips and substrates assembly. The experimental results presented an effective improvement in the die-shear force performance of chips and substrates assembly using the Ar plasma activation. Increasing the die-shear force was attributed to remove the contaminants on the surface of Cu electrodes and Au bumps by the Ar plasma activation. After Au bumps and Cu electrodes were activated by Ar plasma, neither delamination nor crack is found at bonding interface between Au bumps and Cu electrodes for chips and substrates assembly. The die-shear forces were higher than the minimum required value stated in the JEDEC specifications for Cu electrodes and Au bumps with Ar plasma activated. As Cu electrodes with Ar plasma treating under various activated durations, the fracture mode of Au bumps separating from the surface of Cu electrodes transforms to that of Au bumps separating from the bond pads, indicating the bonding strength of Au bumps and Cu electrodes is higher than that of Au bumps and bond pads. A low contact angle was also determined on the surface of Cu electrodes after the Ar plasma activated, indicating a clean bonding surface was achieved. A clear atomic interdiffusion between Au bumps and Cu electrodes was observed for Au bumps and Cu electrodes with Ar plasma activated. The Ar plasma activation was an effective scheme to improve the bonding strength of chips and substrates assembly. Thus, the Ar plasma activation has great potential to be applied to chips and substrates assembly.**

Keywords—argon plasma activation, thermal compression bonding, copper electrode, gold bump.

I. INTRODUCTION

According to bonding energy of chips and substrates assembly, there are three kinds of bonding process, thermal compression, ultrasonic and thermosonic applied to bond chips and substrates. An elevated bonding temperature and a high bonding load are normally required to achieve sound bonds for the thermal compression bonding process. The exceeded high bonding temperature promoted the formation of intermetallic compounds and the thermal stress arose at bonding interface to degrade the bonding quality. A crater easily generates due to high level of the ultrasonic power was applied to bond bumps and electrodes. Thus, the thermosonic boning was widely used in the assembly of chips and substrates, since the thermosonic bonding process combines ultrasonic power and thermal energy to achieve bonding of chips and substrates. However, the ultrasonic power could be absorbed by flex substrates, thus it difficult propagated to the bonding interface to achieve sound bonds for assembly of chips and flex substrates [1]. It is undoubted that to develop a new technology, reducing the bonding temperature or decreasing the level of ultrasonic power to achieve sound bonds in electronic packaging are inevitable.

The plasma activation has been widely used in wafers bonding for microelectronics system application. To achieve diffusion bonding of wafers, an elevated bonding temperature is required since the melting point of the wafer is high [2]. However, the thermal damage or thermal stress would be formed at bonding interface due to a high bonding temperature was applied. Thus, the plasma activation was used to reduce the containments they existed on the bonding surface, and then reduced the required bonding energy [3-6]. Therefore, a sound bond can be achieved with a low bonding temperature and a low level ultrasonic power. Li et. al [7] has point out that Ar plasma was an effective scheme to remove containments they existed on the surface of leadfram. The effectiveness highly depended on the parameters of argon plasma activation, plasma power and activation time. The carbon concentration decreased significantly and oxygen concentration increased after the argon plasma activation, indicating the argon plasma can remove the containments only and the activated surface could oxidize instantaneously. The plasma activation with rolling process also has been successfully used in bond of copper foils and flex substrates [8]. After the flex substrates were treated with argon plasma, and then they were bonding to copper foils using rolling process at room temperature under the vacuum environment. An integrity bond are performed, neither delaminations nor defects were observed at bonding interface. The argon plasma is effectively to improve the bonding quality for copper foils and flex substrates assembly. In this study, the argon plasma was expected to remove the containments on the bonding surface and reduced the bonding barrier between chips and substrates.

II. EXPERIMENTAL PROCEDURE

Specimen Preparation

A gold bond pad was posited on the surface of an alumina (Al_2O_3) substrate with the stencil printing process, and then

gold stud bumps were bumped onto gold pads of an alumina substrate with an automatic stud bump bonder using the bumping parameters reported in an earlier work [9]. After gold stud bumping, the bumped substrate was diced into chips of 1.58^{L} x 0.96^{W} x 0.5^{H} mm^3 in dimension. Each chip contained nine gold stud bumps to form area array bumps as shown in Fig. 1. To prepare the copper electrodes on the alumina substrates, the thickness of 0.1um titanium adhesion layer was first deposited on the alumina substrate and then the copper, nickel and silver layers were deposited using electroplating process. The stacking sequence of the deposited layers on the alumina substrates from bottom to top was Ti/Cu/Ni/Ag. The thickness of the silver bonding layer was 1.2 µm and the nickel barrier layer and copper layer were approximately 0.5µm- and 1.2µm-thick, respectively. A silver layer plated on nickel barrier layer as a bonding layer to improve the bonding strength of chips and substrates assembly.

Chips and Substrates assembly

The physical plasma of an argon gas was conducted to activate the chips and substrates. The major activated parameters were 400 W in power, 140 mTorr in base pressure, 20 Sccm in flow rate of the argon gas. The activated time varied from 10-90s for investigating the effects of the activated time on the bonding strength of chips and substrates assembly. The contact angle was measured to evaluate the effect of the argon plasma activation on substrates. Chips and substrates assembled using thermal compression bonded process for they were activated by argon plasma. Die-shear test was subsequently performed on bonded chip and substrates using a Royce 552 tester according to the procedure specified by EIA/JEDEC JESD22-B116 [10]. The die-shear force was the average force obtained from test results of at least 10 samples for each set of bonding parameters. The diameter of the gold bumps bonded onto the copper electrodes over substrates and the bonding interface between the gold bumps and copper electrodes were investigated using scanning electron microscope (SEM). After die-shear test, the fracture morphology on the chip side and on the substrate side was analyzed using SEM with the energy dispersive spectrometry (EDS).

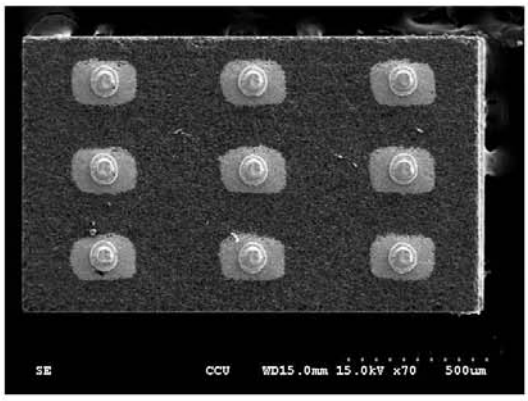

Fig 1. Gold stud bumps thermosonically bonded on pads over chips to form an area array bumps

III. Results and Discussion

Effects of the bonding load on die-shear forces

Bonding load is a critical parameter for chips and substrates assembly using thermal compression bonding process. To verify the bonding load on the die-shear force, the bonding load was varied from 2 kgf to 10 kgf and other bonding parameters were fixed, 200°C in bonding temperature and 20 mins in bonding time. Both gold stud bumps and copper electrodes over substrates were activated with the argon plasma prior to assemble chips and substrates. Diameters of gold bumps bonded on copper electrodes were determined using the SEM to establish the threshold value of die-shear force according to the EIA/JEDEC specifications [9]. Figure 1 presents the effect of the bonding load on the die-shear force of chips bonded on the substrates. The die-shear force increased form 200 gf to 600 gf with an increasing bonding loads in the rage of 2 kgf to 10 kgf. Obviously, the die-shear force was improved by increasing the bonding loads. This improvement of die-shear forces could be attributed by increasing the bonding area between gold bumps and copper electrodes. A value of the minimum required die-shear force depends on the contact diameter of bumps bonded on electrodes specified in EIA/JEDEC specifications.

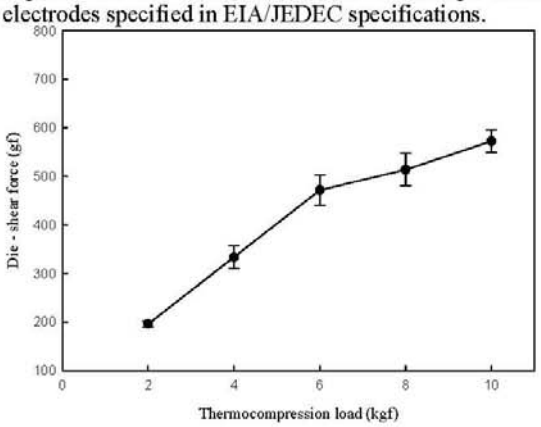

Fig 2. Dis-shear forces of chips and substrates assembly using thermal compression bondign process.

Fig. 3 shows the diameter of gold bumps bonded to copper electrodes with various bonding loads. At low bonding loads of 2 kgf and 4kgf, the contact diameter of gold bumps bonded to copper electrodes was approximately 45.25 µm and 77.78 µm as shown in Figs. 3a and b, respectively. Values of the minimum ball-shear forces specified in the JEDEC specification are approximately 12 gf and 32 gf for ball bond diameters of 45.72 µm (1.8 mil) and 77.8 µm (3.0 mil). For each chip with nine gold bumps, reasonable average die-shear forces of chips and substrates assembly should be at least 108 gf for an bonding load of 2 kgf and 288 gf for an bonding load of 4 kgf. Die-shear forces shown in Fig. 2 are far exceed the minimum required values for chips and substrates assembly using bonding loads of 2 kgf and 4 kgf. As bonding loads increased to 6 kgf and higher, a large deformation is formed, the diameter of gold bumps increases significantly as shown in Figs. 3c and d. According to diameters of gold bumps bonded on copper electrodes, the minimum die-shear forces are 792 gf and 900 gf for bonding loads of 6 kgf and 8 kgf,

respectively. Eperiments obtained in the Fig. 2 depicts that bonding loads of 6 kgf and higher failed to meet the requirements stated in the JEDEC specification. At bonding load of 2 kgf, although the die-shear force is higher than the minimum required stated in JEDEC specification, but this value was low. Hence, the bonding load of 4 kgf is slected in this study.

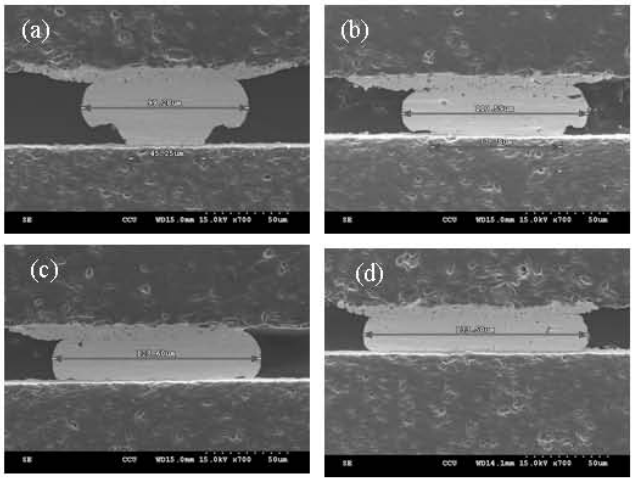

Fig. 3 SEM micrographs of the cross-section of chip bonded onto copper electrodes using various bonding loads, (a) 2kgf, (b) 4kgf, (c) 6kgf, (d) 8kgf. Other bonding parameters: bonding temperature 200°C , bonding time 30 mins.

Effects of Ar plasma actived on die-shear forces

Fig. 4 presents the effects of Ar plasma activated times on die-shear force of chips and substrates assembly. Major parameters of the thermal compression bonding are 4 kgf in bonding load, 200°C in bonding temperature and 20 mins in bonding time. Both gold bumps and copper electrodes without Ar plasma activating, the average die-shear force is 222.6 gf, which is lower than the minimum required value of 288 gf specified in JEDEC specification, indicating this value is insufficient to meet the requirements. A slight enhancement in the die-shear force of 263.9 gf is obtained in Fig. 4 when gold bumps was treated with Ar plasma 30 s and copper electrodes without Ar plasma activated. For gold bumps were activated with Ar plasma 30s, the die-shear force increases with increasing the Ar plasma activated time of copper electrodes form 10 s to 30 s and the die-shear forces are varied in a narrow range for Ar plasma activated time further extended from 60 s to 90 s. All die-shear forces are higher than the minimum required value of 288 gf specified in JEDEC specification when both gold bumps and copper electrodes were treated with Ar plasma. Similar trend of die-shear forces can be found in Fig. 4 for extending Ar plasma activated time of copper electrodes and gold bumps without Ar plasma activated, however, the die-shear forces are below the minimum required value of 288 gf. This experiment result indicates that the Ar plasma activation effectively improved the die-shear force of chips and substrates assembly when they were treated with Ar plasma activation.

To investigate the possible reason for doe-shear forces increasing with the Ar plasma activation, the cross-sections of gold bumps bonded onto copper electrodes were achieved for gold bumps and copper electrodes under various treatments, as shown in Fig. 5. A delamination was found at bonding interface between the gold bump and the copper for gold bumps and copper electrodes without Ar plasma activation as shown in Fig. 5a. For copper electrodes with Ar plasma activation 30 s and gold bumps without treating with Ar plasma, the delamination also was observed at bonding interface, as shown in Fig. 5b. An integrity bonding interface of gold bumps bonded to copper electrodes was revealed in Figs. 5c and d for copper electrodes and gold bumps treating with Ar plasma activation at various activated times. The delamination at bonding interface results a low die-shear force for gold bumps and copper electrodes without Ar plasma activation. This result can be used to explain low die-shear forces were obtained in Fig. 2 for gold bumps and copper electrodes without Ar plasma activation. The containments presence at bonding surface of copper electrodes and gold bumps lead to hinder the atomic interdiffusion between copper electrodes and gold bumps, and then the delamination would form. In contrast to the delamination existing at bonding interface for copper electrodes and gold bumps without Ar plasma activation, an atomic interdiffusion between copper electrodes and gold bumps was promoted for copper electrodes and gold bumps with Ar plasma activation, and then a defect-free bonding interface results in high die-shear force as shown in Fig. 2.

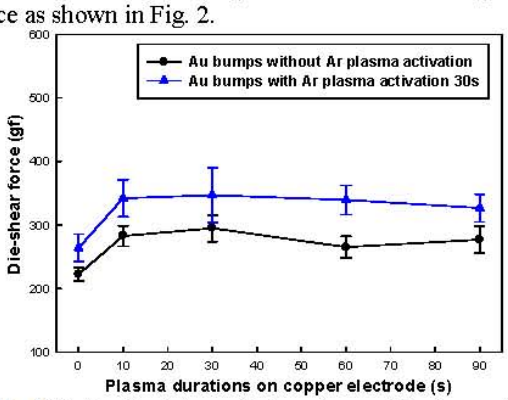

Fig. 4 Relationships between die-shear force and Ar plasma activation time on copper electrodes.

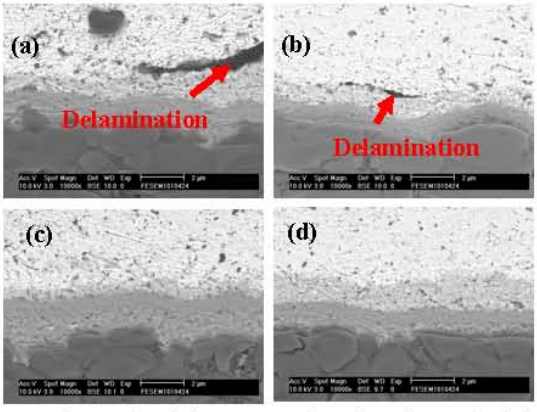

Fig. 5 SEM micrographs of the cross-section of Au bumps bonded to Cu electrodes for (a) Cu electrodes and Au bumps without Ar plasma activated, (b) copper electrodes with Ar plasma activated 30s and Au bumps without Ar plasma activated, (c) Cu electrodes with Ar plasma activated 10s and Au bumps with Ar plasma activated 30s, (d) Cu electrodes and Au bumps with Ar plasma activated 30s.

After the die-shear test, fracture modes of specimens were divided into two categories, gold bumps separated from the surface of bond pads at chip side and gold bumps separated from the surface of copper electrodes at substrate side. The facture mode of gold bumps separated at chip side indicating the bonding strength of gold bumps and copper electrodes was higher that gold bumps and bond pads on chips. Thus, the fracture modes implies that die-shear forces depends on the bonding conditions of gold bumps and copper electrodes. To analyze changes in fracture modes under various Ar plasma activation on gold bumps and copper electrodes, fracture mode of each bump was calculated and plotted as shown in Fig. 6. Both gold bumps and copper electrodes without Ar plasma activation, the main fracture mode is gold bump separated from the surface of copper electrodes, indicates the bonding strength of gold bumps and copper electrodes was poor. For gold bumps without Ar plasma activation and copper electrodes with Ar plasma treating at various activating times, most of gold bumps separated from the surface of copper electrodes, implying the bonding strength of gold bumps and copper electrodes is lower than that of gold bumps and bond pads as shown in Fig.6a. Fig. 6b presents that the main fracture mode is gold bumps separating from the surface of copper electrodes for gold bumps with Ar plasma activating 30 s and copper electrodes without Ar plasma activating. As copper electrodes with Ar plasma treating under various activated times, the fracture mode of gold bumps separating from the copper electrodes transforms to that of gold bumps separating from the bond pads, indicating the bonding strength of gold bumps and copper electrodes is higher than that of gold bumps and bond pads. These results are consistent with the changes in die-shear forces. These experimental results are consisted with changes in die-shear forces as shown in Fig. 2.

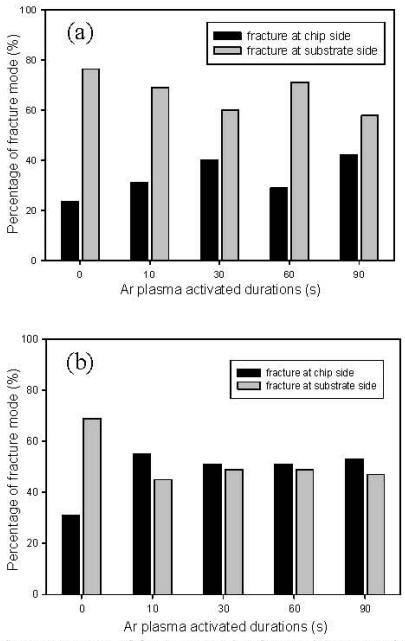

Fig. 6 The percentage of fracture modes for Au bumps and Cu electrodes treating with Ar plasma under different conditions, (a) only Cu electrodes with Ar plasma activation, (b) both Au bumps and Cu electrodes with Ar plasma activation.

Surfce compositions of Cu electrodes and Au bumps afetr Ar plasma activation

The compositions on the surface of copper electrodes were determined using Auger spectrometry for they were treated with Ar plasma at various durations, as shown in Fig. 7. For copper electrodes without Ar plasma activated, the main component on the surface of copper electrodes was silver and carbon, and small amount of oxygen and sulfur as shown in Fig. 7a. A small amount of sulfur on the surface of copper electrodes would be the residue during electroplating silver bonding layer. As copper electrodes with Ar plasma activated, the percentage of silver increased with the activated durations and the carbon was decreased, as shown in Fig. 7a. The Ar plasma activation removed the containments on the surface of copper electrodes and a high percentage of silver thus can be obtained. This experimental result can be used to explain the high die-shear force was achieved for copper electrodes treating with Ar plasma. No significant change in the percentage of oxygen was found in Fig. 7a. Since the Ar is an inert gas, no oxidation or reduction reactions would occur, the percentage of oxygen maintain in the range of 2.83% to 3.14% approximately. Similar results also observed in Fig. 7b for gold bumps treating with Ar plasma under various activation durations. The percentage of gold increased and the carbon decreases after gold bumps with Ar plasma activated 30 s, indicating the containments on the surface of gold bumps was removed by Ar plasma activation. Both gold bumps and copper electrodes with Ar plasma activation, the containments on the bonding interface of gold bumps and copper electrodes were lowest among the only copper electrodes with Ar plasma activation and both of them without treating with Ar plasma. As a result, the maximum die-shear force was achieved for copper electrodes and gold bumps with Ar plasma activation as shown in Fig 2.

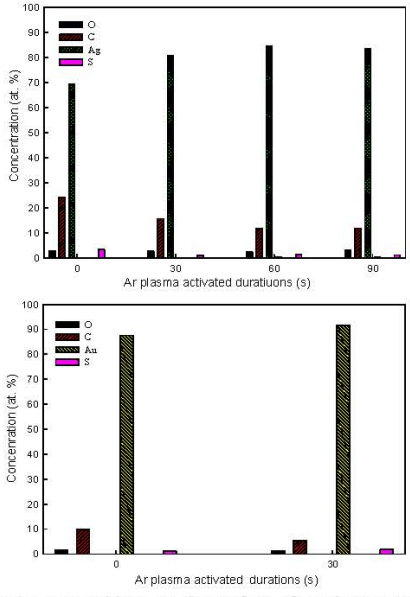

Fig. 7 The compositions on the surface of Au bumps and Cu electrodes under various conditions , (a) Cu electrodes treating with Ar plasma under activated durations from 0-90 s, (b) Au bumps with Ar plasma under activated durations from 0-30 s.

The contact angle was an index to express the wettability of bonding materials. Containments on the surface of bonding materials result in high contact angle, implying the wettability of bonding materials was poor. Thus, the contact angle can be used to evaluate the cleanness of bonding materials. Fig. 8a shows a high contact angle of 96.94° was obtained for copper electrodes without Ar plasma activation and a low contact angle of 51.88° shown in Fig. 8b was achieved for copper electrodes treating with Ar plasma 10 s. As extending the Ar plasma activated durations, the contact angles did not decrease and varied in a small range of 51-56° as shown in Figs. 8c and d. According to analytical results on the compositions of copper electrodes shown in the Fig. 7, this phenomenon would attribute to the oxide on the surface of copper electrodes and it can't be removed by Ar plasma.

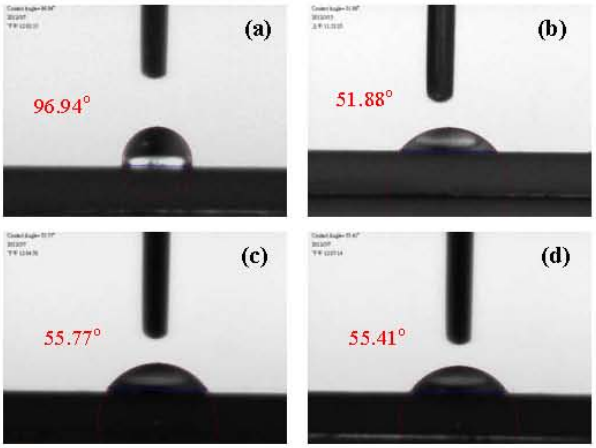

Fig. 8 The contact angle measured on the surface of copper electrodes under various conditions, (a) copper electrodes without Ar plasma activation, (b) copper electrodes with Ar plasma activated 10 s, (c) copper electrodes with Ar plasma activated 30 s, (d) copper electrodes with Ar plasma activated 90 s.

The containments and the contact angle on the surface of copper electrodes decreased significantly for copper electrodes with Ar plasma activated, indicating the wettability of copper electrodes with Ar plasma activated was enhanced. Both copper electrodes and gold bumps with Ar plasma activated, the die-shear forces of chips and substrates assembly were higher than the minimum required value stated in the JEDEC specification as shown in Fig. 2. The Ar plasma activation is an effectively scheme to remove the containments on the surface of copper electrodes and gold bumps, and atomic interdiffusion between gold bumps and copper electrodes was enhanced, and then the bonding strength of chips and substrates assembly was improved.

Effects of Ar plasma activation on the bondign interface

To investigate the integrity of the bonding interface between gold bumps and copper electrodes, a field-emission Auger electronic spectroscopy (FEAES) was applied to determine the atomic interdiffusion at bonding interface. For copper electrodes and gold bumps with Ar plasma activated, a sound bond was achieved and no delaminations or voids were observed at the bonding interface between gold bumps and copper electrodes as shown in Fig. 9a. The obvious atomic interdiffusion between the gold bump and silver bonding layer on the copper electrodes was obtained as shown in Fig. 9b. Based on theses experimental result, the strengthen mechanism of Ar plasma activation on chips and substrates assembly can be proposed. After Ar plasma activated, the containments in the bonding interface of gold bumps and copper electrodes were removed, the diffusion barrier was reduced, and then the atomic interdiffusion was improved during thermal compression bonding, finally the bonding strength of chips and substrates assembly were enhanced.

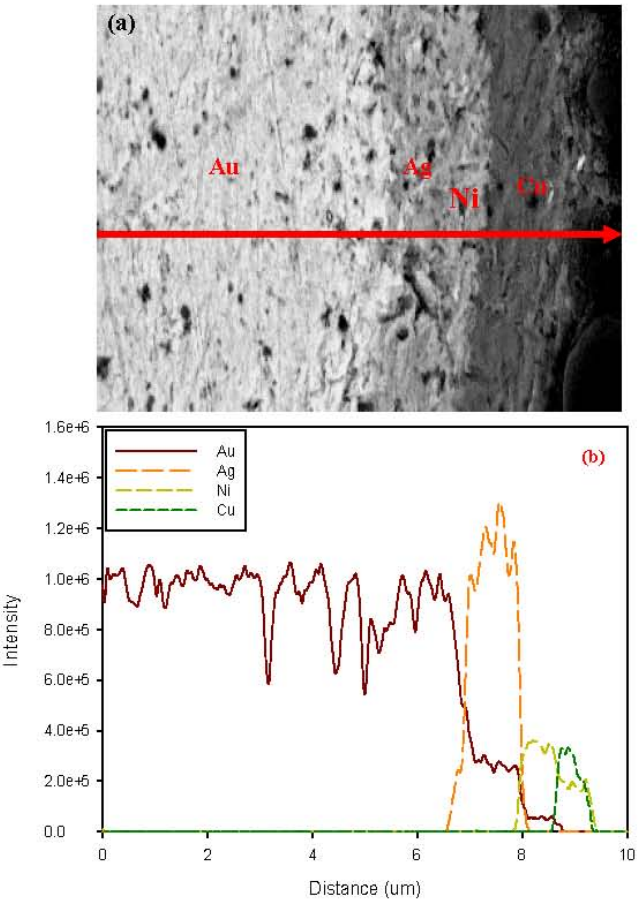

Fig. 9 (a) The cross-section of Au bump bonded on copper electrode after gold bumps and Cu electrodes were activated with Ar plasma, (b) line scanning profile of the bonding interface between the Au bump Cu electrode after gold bumps and Cu electrodes were activated with Ar plasma.

IV. Conclusions

For gold bumps and copper electrodes with Ar plasma activated, the die-shear force of chips and substrates assembly using the thermal compression bonding process was improved. A sound bond with sufficient bonding strength can be achieved. Neither delamination nor other defect was found at bonding interface. The main fracture mode was gold bumps separated from the bond pads on chip side after die-shear test

for gold bumps and copper electrodes were activated with Ar plasma , indicating the bonding strength at bonding interface of gold bumps and copper electrodes was higher than that of gold bumps and bond pads. Based on the experimental results, the Ar plasma activation is an effective scheme to improve the bonding strength of chips and substrates assembly during the thermal compression bonding process.

It also can be found that a low contact angle was obtained for copper electrodes with Ar plasma activated, implying the surface of copper electrodes with a better good performance of wettability than that without Ar plasma activated. A low level of containments on the surface of copper electrodes and gold bumps can be achieved for gold bumps and copper electrodes treating with Ar plasma. The cleanliness of bonding interface was enhanced, and then the bonding barrier was reduced, the atomic interdiffusion between gold bumps and copper electrodes was promoted, finally the bonding strength of chips and copper electrodes was improved. Thus, the Ar plasma activation has great potential to be applied to chips and substrates assembly with the compression bonding process.

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[10] JEDEC Standard, EIA/JESD22-B-116, ''Wire Bond Shear Test'', 1998.

四、建議

觀察中國研究模式大部分屬團隊方式，以校系或研究中心為主體，集合各種領域教師或技術人員從事完整的研究，此一研究模式較容易產出功能性完整之產品或製程技術，除較容易取得大型研究計畫，擁有完整研究設備外，建構完整技術亦可獲得業界信賴，學界與業界之配合較為緊密。此外，中國對半導體上游與下游之構裝技術均投入大筆研究經費或獎助具潛力之公司，促使構裝技術層次推進相當快速，部分大學實驗室可獨立進行 3-D 晶片封裝，上海大學甚至建構封裝研究中心，各式封裝設備依目前業界使用之設備建構，設備相當完整，該實驗結果與業界連動快速，亦能獲得相關業者於研究經費之支持，形成正面且良性循環，明顯有助於提升電子構裝之技術層次，建議國內對相關領域應集中研究資源，籌設共同研究實驗室，功能類似目前科技部所轄之貴儀中心設備，可提供該領域研究所需之設備，對提升研究品質與建立新式製程技術應有所助益。

五、攜回資料名稱及內容

1.ICEPT 2014 Conference Program.
2. SEMICONDUCTOR MANUFACRURING (ISSN:1555-9270)
3.ICEPT 2014 Proceedings (flash disk)
4. EQUIPMENT FOR ELECTRONIC PRODUCTS MANUFACTURING (ISSN:1004-4507)

六、參加會議相關照片

圖一、會議中參加開幕與專家學者演講照片。

圖二、會議中參加分組論文發表照片。

圖三、會議中參加分組論文發表照片。

科技部補助計畫衍生研發成果推廣資料表

日期:2014/10/22

科技部補助計畫	計畫名稱: 以表面活化技術提高非導電膠接合矽晶片與軟性基板之接合強度與可靠度
	計畫主持人: 莊正利
	計畫編號: 102-2221-E-040-005- 學門領域: 加工與製造

無研發成果推廣資料

102 年度專題研究計畫研究成果彙整表

計畫主持人：莊正利	計畫編號：102-2221-E-040-005-
計畫名稱：以表面活化技術提高非導電膠接合矽晶片與軟性基板之接合強度與可靠度	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	1	1	100%		
		研討會論文	1	1	100%		發表於 2014 機械年會。
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	2	1	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	1	100%	篇	稿件正撰寫中，預計年底投寄。
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	1.協助暉盛科技公司探討氬氣電漿活化於軟性基板之適合參數，並由接觸角之量測結果反映低壓活設備之調整參考依據。 2.協助福懋科技公司於電子構裝製程之除錯與接合試片之分析。

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

科技部補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：□已發表 □未發表之文稿 ■撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：（以 100 字為限）

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

1.成功以熱壓覆晶接合製程與非導電膠將晶片接合於軟性基板之製程開發，晶片金凸塊可與軟性基板表面之電極直接接合，形成有效之電訊通路。

2.建立氫氣電漿活化技術對提升晶片與軟性基板接合強度之機制，並探討氫氣電漿活化相關參數對晶片與軟性基板接合強度之影響。

3.部分實驗結果已撰寫成論文發表於 2014 機械年會，完整研究結果目前已著手撰寫成英文稿件，預計年底前投稿至 Surface and Coatings Technology 國際期刊。

4.本研究結果對電子封裝業界於晶片與軟性基板之接合具廣大應用潛力。